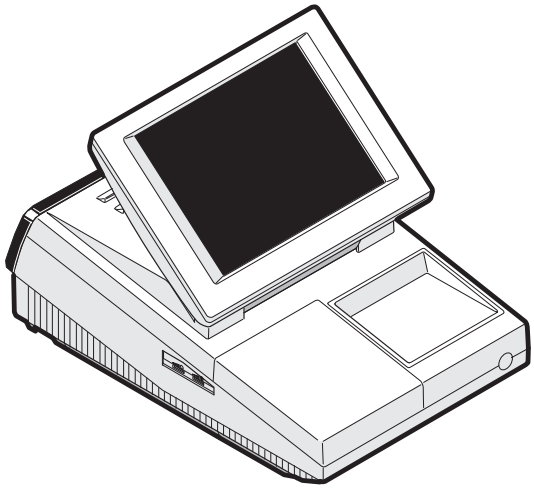
SHARP SERVICE MANUAL

CODE : 00ZUP3301VS2E



POS TERMINAL

MODEL UP-3301

(For "V" version)

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PARTS GUIDE

Parts marked with "⚠" are important for maintaining the safety of the unit. Be sure to replace these parts with specified ones for maintaining the safety and performance of the unit.

SHARP CORPORATION

This document has been published to be used for after sales service only.
The contents are subject to change without notice.

CAUTION

RISK OF EXPLOSION IF BATTERY IS REPLACED
BY AN INCORRECT TYPE.
DISPOSE OF USED BATTERIES ACCORDING
TO THE INSTRUCTIONS.

AVOID: SHORT-CIRCUITING THE BATTERY TERMINALS.
KEEP THE BATTERY AWAY FROM FIRE.

* WHEN DISPOSING THE BATTERY, FOLLOW THE LOCAL
RULES AND REGULATIONS.

"BATTERY DISPOSAL"

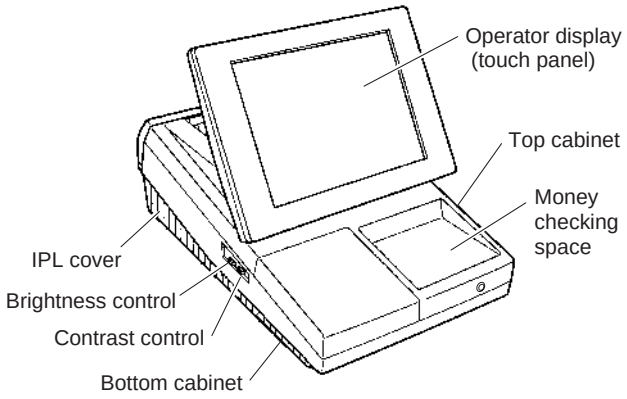
THIS PRODUCT CONTAINS NICKEL-METAL HYDRIDE BATTERY.
THIS BATTERY MUST BE DISPOSED OF PROPERLY.
REMOVE THE BATTERY FROM THE PRODUCT AND CONTACT FEDERAL OR
STATE ENVIRONMENTAL AGENCIES FOR INFORMATION ON RECYCLING AND
DISPOSAL OPTIONS.

CHAPTER 1. SPECIFICATIONS

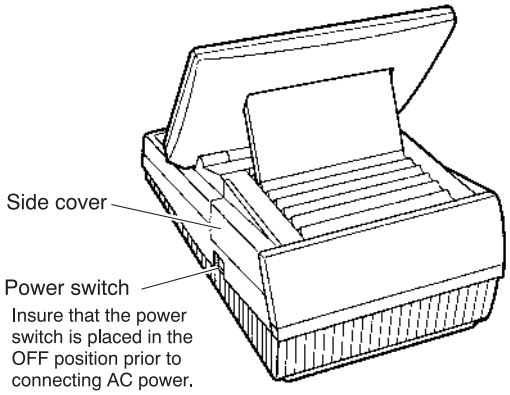
1. Appearance

External view

Front view



Rear view



2. Rating

External dimensions	11.6(W) x 16.3(D) x 12.6(H) in. (295(W) x 414.5(D) x 320(H) mm)
Weight	14.6 lbs. (6.6 kg)
Power source	120V AC ± 10% 60 Hz
Power consumption	Stand-by: 27W Operating: 51W (max.)
Working temperatures	32 to 104°F (0 to 40°C)

3. Displays

This POS terminal is equipped with a color LCD operator display.

The operator display is a touch panel.

The operations can be performed by touching the screen (that shows keys or items in the receipt window) of the operator display.

1) Operator display (touch panel)

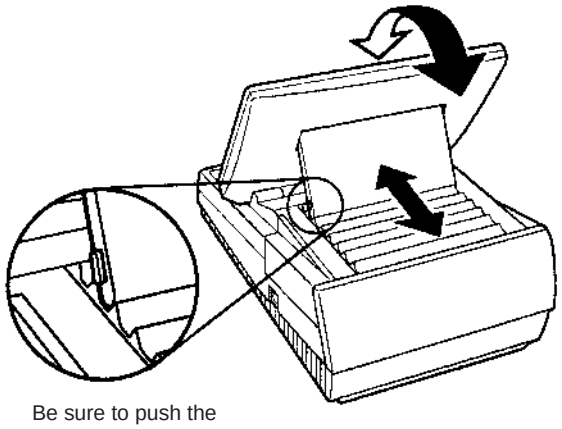
3-1. Display

1) Front display

ITEM	SPECIFICATIONS	NOTE
Type	DSTN color LCD with back light	With 256 colors*
Screen size	10.4” Full screen	
Dot format	640 (W) x 480 (H) mm Full dot	
Dot size	0.09 x RGB(W) x 0.31 mm	
Dot space	0.02 mm	

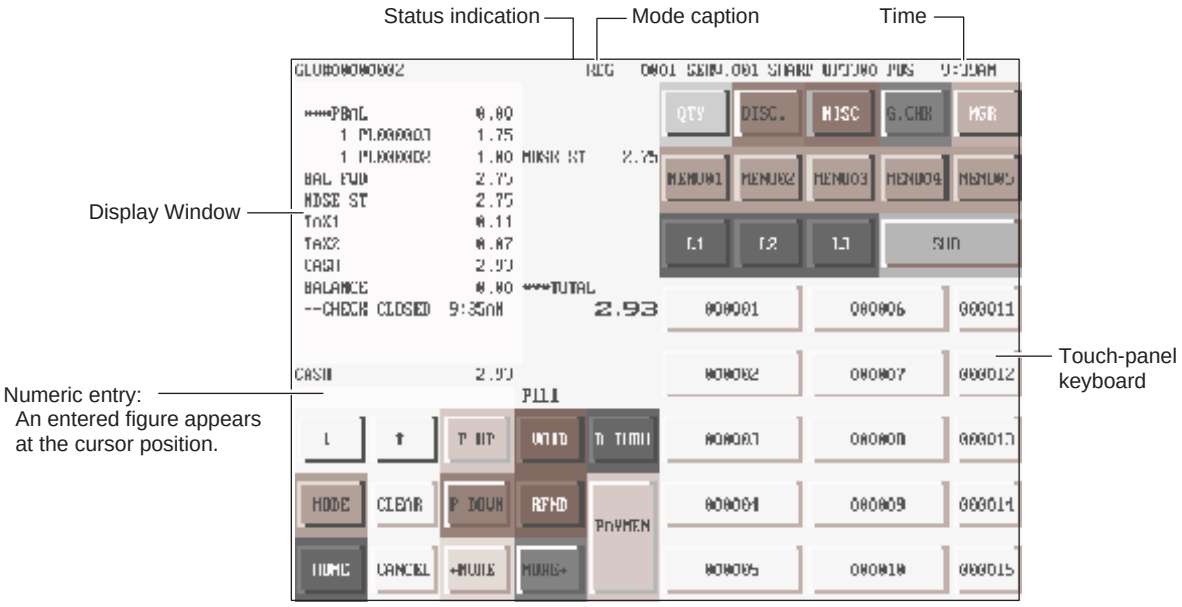
* Note that the application software for the UP-3301 uses 16 colors.

The display can be tilted to the best viewing angle by sliding the rear stand.



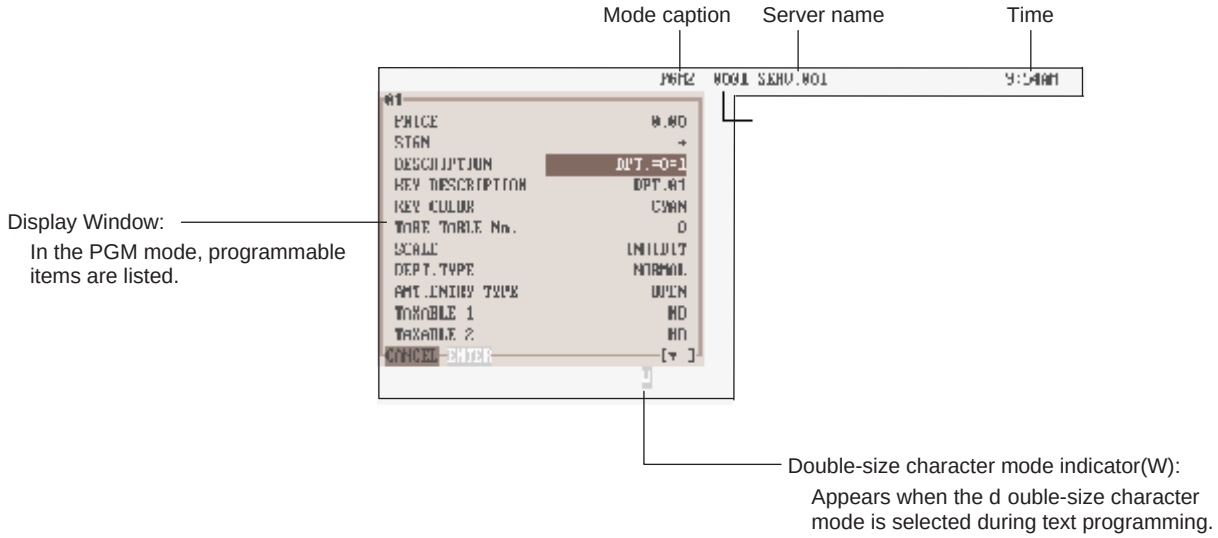
Be sure to push the button on the rear stand when sliding it.

Screen example (REG mode)

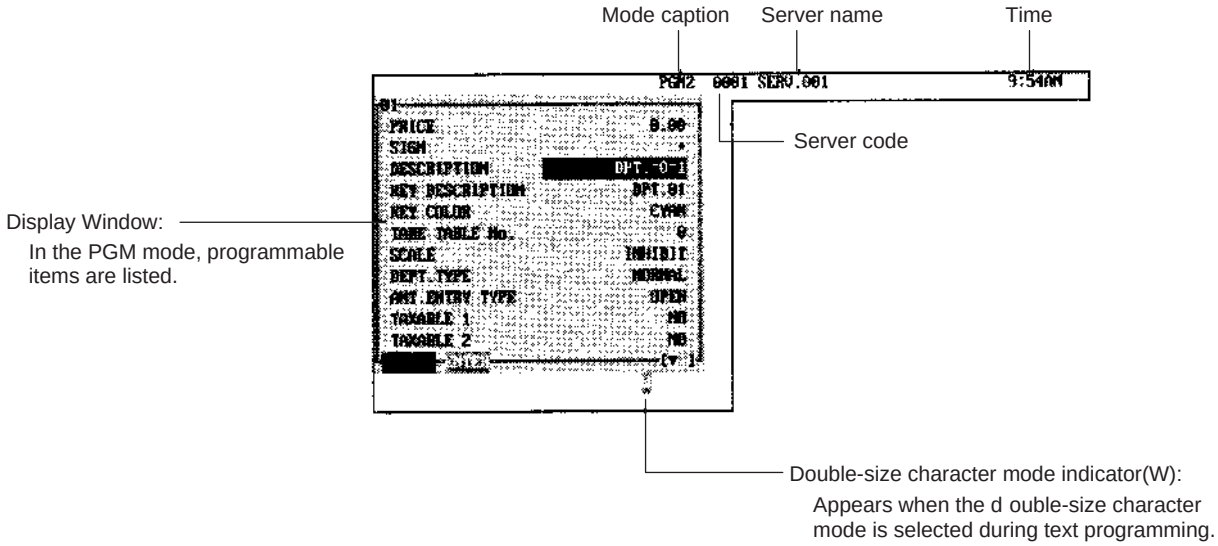


Note: The size of a display area depends on the layout of a touch-panel keyboard (ex. key size) or the function mode (ex. drive-through function).

Display example 1 (REG mode)


Mode caption
Server name
Time
Display Window:
In the PGM mode, programmable items are listed.
Double-size character mode indicator(W):
Appears when the d ouble-size character mode is selected during text programming.

Display example 2 (PGM mode)


Mode caption
Server name
Time
Server code
Display Window:
In the PGM mode, programmable items are listed.
Double-size character mode indicator(W):
Appears when the d ouble-size character mode is selected during text programming.

Keyboard layout (default)

• Home keyboard

This keyboard appears when you touch the [HOME] key.

					QTY	DISC.	MISC	G.CHK	MGR
					MENU01	MENU02	MENU03	MENU04	MENU05
					L1	L2	L3	SUB	
					000001		000006		000011
					000002		000007		000012
↓	↑	P UP	VOID	D-THRU	000003		000008		000013
MODE	CLEAR	P DOWN	RFND	PAYMEN	000004		000009		000014
HOME	CANCEL	←MORE	MORE→		000005		000010		000015

• Main2 keyboard

This keyboard appears when you touch the [MORE→] key on the Home keyboard.

					QTY	DISC.	MISC	G.CHK	MGR
					MENU01	MENU02	MENU03	MENU04	MENU05
					L1	L2	L3	SUB	
					000016		000021		000026
					000017		000022		000027
↓	↑	P UP	VOID	D-THRU	000018		000023		000028
MODE	CLEAR	P DOWN	RFND	PAYMEN	000019		000024		000029
HOME	CANCEL	←MORE	MORE→		000020		000025		000030

• Main3 keyboard

This keyboard appears when you touch the [MORE→] key on the Main2 keyboard.

					QTY	DISC.	MISC	G.CHK	MGR
					MENU01	MENU02	MENU03	MENU04	MENU05
					L1	L2	L3	SUB	
					000031		000036		000041
					000032		000037		000042
↓	↑	P UP	VOID	D-THRU	000033		000038		000043
MODE	CLEAR	P DOWN	RFND	PAYMEN	000034		000039		000044
HOME	CANCEL	←MORE	MORE→		000035		000040		000045

• Sub keyboard

This keyboard appears when you touch the [SUB] key on the Home keyboard.

					P1	P2	P3	P4	P5
					COMB01		COMB06		000101
					COMB02		COMB07		000102
					COMB03		COMB08		000103
					COMB04		COMB09		000104
↓	↑	P UP	VOID		COMB05		COMB10		000105
MODE	CLEAR	P DOWN	RFND	PAYMEN				WAIT	
HOME	CANCEL	MORE→						FINAL	

• Sub2 keyboard

This keyboard appears when you touch the [MORE→] key on the Sub keyboard.

					P1	P2	P3	P4	P5
					COMB11		COMB16		000106
					COMB12		COMB17		000107
					COMB13		COMB18		000108
					COMB14		COMB19		000109
↓	↑	P UP	VOID	SUB	COMB15		COMB20		000110
MODE	CLEAR	P DOWN	RFND	PAYMEN				WAIT	
HOME	CANCEL	←MORE						FINAL	

• Sub3 keyboard

This keyboard appears when you touch the [MORE→] key on the Sub2 keyboard.

↓	↑	P UP	VOID	SUB					
MODE	CLEAR	P DOWN	RFND	PAYMEN					
HOME	CANCEL	←MORE	MORE→						

• Condiment/Menu keyboard

This keyboard appears when you touch the MENU key in a condiment PLU entry.

The Condiment/Menu2 keyboard appears when you touch the [MORE→] key on the Condiment/Menu keyboard.

The Condiment/Menu3 keyboard appears when you touch the [MORE→] key on the Condiment/Menu2 keyboard.

					KEY001		KEY006		KEY011
					KEY002		KEY007		KEY012
					KEY003		KEY008		KEY013
					KEY004		KEY009		KEY014
					KEY005		KEY010		KEY015
↓	↑	P UP	VOID	SUB					
MODE	CLEAR	P DOWN	RFND	PAYMEN				WAIT	
HOME	CANCEL	C NEXT			MORE→			FINAL	

• Function menu 1 (QTY) keyboard

This keyboard appears when you touch the [QTY] key on the Home, Main2, or Main3 keyboard.

					X/TIMES				
					7	8	9		
					4	5	6		
↓	↑	P UP			1	2	3		
MODE	CLEAR	P DOWN			0	00	-		
HOME	CANCEL				X/TIMES				

• Function menu 2 (DISC.) keyboard

This keyboard appears when you touch the [DISC.] key on the Home, Main2, or Main3 keyboard.

					%1		%5	(-)3	
					%2		%6	(-)4	
					%3		(-)1	(-)5	
					%4		(-)2	(-)6	
					7	8	9	MDS ST	
↓	↑	P UP	VOID	SUB	4	5	6		
MODE	CLEAR	P DOWN	RFND	PAYMEN	1	2	3	MDS ST	
HOME	CANCEL	M.FUNC			0	00	-	PAYMENT MENU	

• Function menu 3 (MISC) keyboard

This keyboard appears when you touch the [MISC] key on the Home, Main2, or Main3 keyboard.

					TAX1SF	RLU/SB		WASTE	
					TAX2SF	RCP.SW		REPEAT	
					TAX	RCPT		RP SND	
					SRV#		MGR#		
					7	8	9		
↓	↑	P UP	VOID	SUB	4	5	6		
MODE	CLEAR	P DOWN	RFND	PAYMEN	1	2	3		
HOME	CANCEL	D-THRU			0	00	-	ENTER	

• Function menu 4 (G.CHK) keyboard

This keyboard appears when you touch the [G.CHK] key on the Home, Main2, or Main3 keyboard.

					QTY	DISC.	MISC		MGR
					SRV#		MGR#		
					7	8	9	N.C.	
↓	↑	P UP	VOID	SUB	4	5	6	CVCNT	
MODE	CLEAR	P DOWN	RFND	PAYMEN	1	2	3	PBAL	
HOME	CANCEL	MFUNC			0	00	-	ENTER	

• Function menu 5 (MGR) keyboard

This keyboard appears when you touch the [MGR] key on the Home, Main2, or Main3 keyboard.

					EMPL#		SRV#		M.FUNC
					E.SALE		TIME-IN		WASTE
					BAL		TIME-OUT		#
					MGR#		BREAK		NS
					7	8	9	SBTL	
↓	↑	P UP	VOID	RCP.SW	4	5	6	PAYMENT MENU	
MODE	CLEAR	P DOWN	RFND	RCPT	1	2	3	ENTER	
HOME	CANCEL	RETURN	ST VD	BILL	0	00	-	CASH	

• Function menu 6 or Function menu 7 keyboard

This keyboard appears when you touch the [FUNC.6] or [FUNC.7] key on the Home, Main2, or Main3 keyboard.

↓	↑	P UP							
MODE	CLEAR	P DOWN							
HOME	CANCEL								

• Payment menu (PAYMENT MENU) keyboard

This keyboard appears when you touch the [PAYMENT MENU] key on the Home, Main2, or Main3 keyboard.

					QTY	DISC.	MISC	WAIT	
					CH1		EAT IN1	FINAL	
					CH2		EAT IN2	$5	
					CH3		EAT IN3	$10	
					7	8	9	$20	
↓	↑	P UP	VOID	SUB	4	5	6	NEXT$	
MODE	CLEAR	P DOWN	RFND	M.FUNC	1	2	3	SBTL	
HOME	CANCEL	STVOID			0	00	-	CASH	

• Drive thru (D-THRU) keyboard

This keyboard appears when you touch the [D-THRU] key on the Home, Main2, or Main3 keyboard.

↓	↑			N.C.2	WAIT
MODE	CLEAR			PBAL2	RECALL
HOME	CANCEL			SUB	ENTER

• SRV/PGM/XZ mode keyboard

This keyboard appears when you touch the [MODE] key on the Home, Main2, or Main3 keyboard.

					↑	P UP	MODE	AUTO21	
					↓	P DOWN	LIST	AUTO22	
					EMPL#		CANCEL	AUTO23	
					SRV#	X/TIME	CLEAR	AUTO24	
					7	8	9	AUTO25	
					4	5	6	NEXT	HOME
		UPDATE	PREV	CALL	1	2	3	ENTER	
		INS	DEL	BKSPC	0	00	-	CASH	

These keys will not appear in the OPXZ,X1,Z1,X2, or Z2 mode.

• Character keyboard

This keyboard is used when you need to enter text data during PGM2 mode entries.

					INS	DEL	P.DW	↑	P.UP
					PREV	NEXT	←	↓	→
					CANCEL	B.S	DC		CODE
					CLEAR				
					ENTER				
								→/←	↑/↓
					_/+	-/=	;/:	[/{	]/}
1/!	2/@	3/#	4/$	5/%	6/^	7/&	8/*	9/(	0/)
q/Q	w/W	e/E	r/R	t/T	y/Y	u/U	i/I	o/O	p/P
a/A	s/S	d/D	f/F	g/G	h/H	j/J	k/K	l/L	
z/Z	x/X	c/C	v/V	b/B	n/N	m/M	,/<	./>	//?
SHIFT			SPACE				SHIFT		

Function keys list (default keyboard and labels)

Caption (default)	Function
HOME	Used to return to the HOME keyboard.
CANCEL	Used to cancel your current operation or menu or return to the previous menu.
CLEAR	Used to clear the entered data (amounts/rates/ parameters, etc.) and the error state.
MODE	Used to go to the MODE selection window or to return to the HOME keyboard.
↑	Used to control the cursor (up arrow).
↓	Used to control the cursor (down arrow).
← MORE	Used to change the keyboard.
→ MORE	Used to change the keyboard.
ENTER	Used to select item/menu or entered data.
SUB	Used to go to the sub-keyboard.
CASH	Used to enter the direct cash/amount tendered operation, or to finalize the PGM job.
0 thru 9	Used to enter a numeric data (0 thru 9).
00	Used to enter a numeric data (00).
000	Used to enter a numeric data (000).
•	Used to enter a fractional part, or to toggle between two or more options.
X/TIMES	Used to enter a quantity or time.
SBTL	Used to display subtotals.
P UP	Used to scroll page up.
P DOWN	Used to scroll page down.
BKSPC	Used to backs up the cursor for deleting the character or figure at the left of the cursor.
DEL	Used to delete a character or figure in the cursor position.
MDS ST	Used to display the merchandise subtotal.
TRY ST	Used to display the tray subtotal.
#	Used to enter a non-add code.
NS	Used to execute a no-sale function.
SCALE	Used to enter a weight for an item entry.
PLU/SB	Used to enter a PLU/subdepartment from the list by using a PLU code.
L1 thru L10	Used to shift the direct PLU key level (level 1 thru 10).
P1 thru P5	Used to shift the PLU price level (level 1 thru 5).
TAX1SF	Used to shift the taxability for tax-1.
TAX2SF	Used to shift the taxability for tax-2.
TAX3SF	Used to shift the taxability for tax-3.
TAX4SF	Used to shift the taxability for tax-4.
BILL	Used to print the bill.
RCPT	Used to print the receipt after transaction.
CH TIP	Used to enter the charge tip.
CA TIP	Used to enter the cash tip.
TIP PD	Used to execute the tip paid function.
VOID	Used to void a last item, or used for the cursor void function.
I.VOID	Used to void a past item, or used for the cursor void function.
ST VD	Used to void an entire transaction (subtotal void).
RFND	Used to enter the refund item.
RETURN	Used to enter the returned item.

Caption (default)	Function
%1 thru %9	Used to enter the percent calculation (percent 1 thru 9).
(–)1 thru (–)9	Used to execute the discount entry (discount 1 thru 9).
TAX	Used to enter the manual tax.
CV CNT	Used to enter the cover count.
AUTO to AUTO7	Used to enter the automatic sequencing (auto 1 thru auto 7).
$5	Used to enter the speed tender ($5).
$10	Used to enter the speed tender ($10).
$20	Used to enter the speed tender ($20).
AUTO11 to AUTO25	Used to enter the automatic sequencing (auto 11 thru auto 25).
CA2	Used to enter the cash 2 payment.
CHK thru CHK4	Used to enter the check payment (check 1 thru 4).
CH1 thru CH8	Used to enter the charge payment (charge 1 thru 8).
EMP CH	Used to enter the employee charge payment.
CONV1 to CONV4	Used to creates a subtotal in foreign currency (conversion 1 thru 4).
PBAL	Used to lookup the guest check.
PBAL2	Used to lookup the guest check (for drive-thru function).
N.C.	Used to open a new guest check.
N.C.2	Used to open a new guest check (for drive-thru function).
SRVC	Used to finalize the guest check temporarily.
FINAL	Used to finalize the guest check temporarily (with the tax calculation).
DEPO	Used to enter the deposit.
DEP.RF	Used to return the deposit.
B.T.	Used to enter the bill transfer/bill totalizing.
RA and RA2	Used to enter the received-on-account (RA 1 and 2).
PO and PO2	Used to enter the paid-out (PO 1 and 2).
SRV#	Used to enter the server code.
MGR#	Used to enter the manager code.
EMPL#	Used to enter the employee code.
EATIN1 thru EATIN3	Used to display the eat-in subtotal (eat-in 1 thru 3).
RP SND	Used to send a partial order to the remote printer.
GRT EX	Used to exempt a customer from the gratuity.
OPN TR	Used to enter the open tare.
BAL	Balance key
REPEAT	Used to repeat a last item entry.
TR.OUT	Used to enter the transfer-out function.
TR.IN	Used to enter the transfer-in function.
PERSN#	Used to enter the person number.
I.PAY	Individual payment key
E.SALE	Used to enter the sales for employees.
M.FUNC	Used to display the miscellaneous function menu.
RCP.SW	Used to switch the receipt printing state (ON/OFF).
WAIT	Used to shift the corresponding guest check to the wait mode (for drive-thru).

Caption (default)	Function
RECALL	Used to re-call the corresponding guest check to the registration mode (for drive-thru).
B.S.	Used to separate the bill.
WASTE	Used to enter/release the WASTE mode.
C NEXT	Used to skip the next table of condiments.
TIME-IN	Used to enter time-in operation.
TIME-OUT	Used to enter time-out operation.
BREAK	Used to enter Break-in/out operations.
QTY	Used to go to the function menu 1 keyboard (q'ty entry).
DISC.	Used to go to the function menu 2 keyboard (discount/percentage entry).
MISC	Used to go to the function menu 3 keyboard (the miscellaneous function keyboard).
G.CHK	Used to go to the function menu 4 keyboard (guest check entry).
MGR	Used to go to the function menu 5 keyboard (Manager/Server/Employee entry).
FUNC.6	Used to go to the function menu 6 keyboard (empty).
FUNC.7	Used to go to the function menu 7 keyboard (empty).
PAYMENT MENU	Used to go to the payment menu keyboard.
D-THRU	Used to go to the drive-thru menu keyboard (guest check entry for drive-thru).
NEXT$	Used to enter the next high-dollars (for including-tax subtotal).
MENU01 to MENU50	Used for PLU menu items (menu 1 thru 50).

2) Customer display

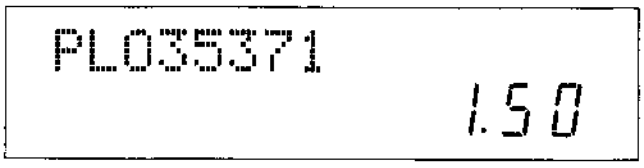
The customer display consists of a 16-position dot-matrix display (upper) and a 11-position 7-segment display (lower).

Lower line

ITEM	SPECIFICATIONS	NOTE
Type	7 Segment type	
Number of digits	11 digits	
Color display	Green	
Character size	12.0(H) x 6.0(W)mm,	

Upper line

ITEM	SPECIFICATIONS	NOTE
Type	Dot matrix type	
Number of digits	16 digits	
Color display	Green	
Character size	9.0(H) x 5.6(W)mm,	

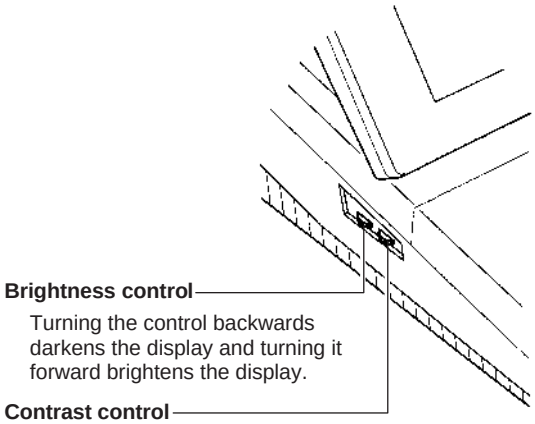


3) Screen save mode

To save electrical power or the display's life, your POS terminal is provided with the screen save function. This function can turn the LCD backlight off when the POS terminal is left idle for an extended period of time. You can program the time for which your POS terminal should keep the normal status (in which the backlight is "ON") before it goes into the screen save mode.
To exit the screen save mode, touch a key.

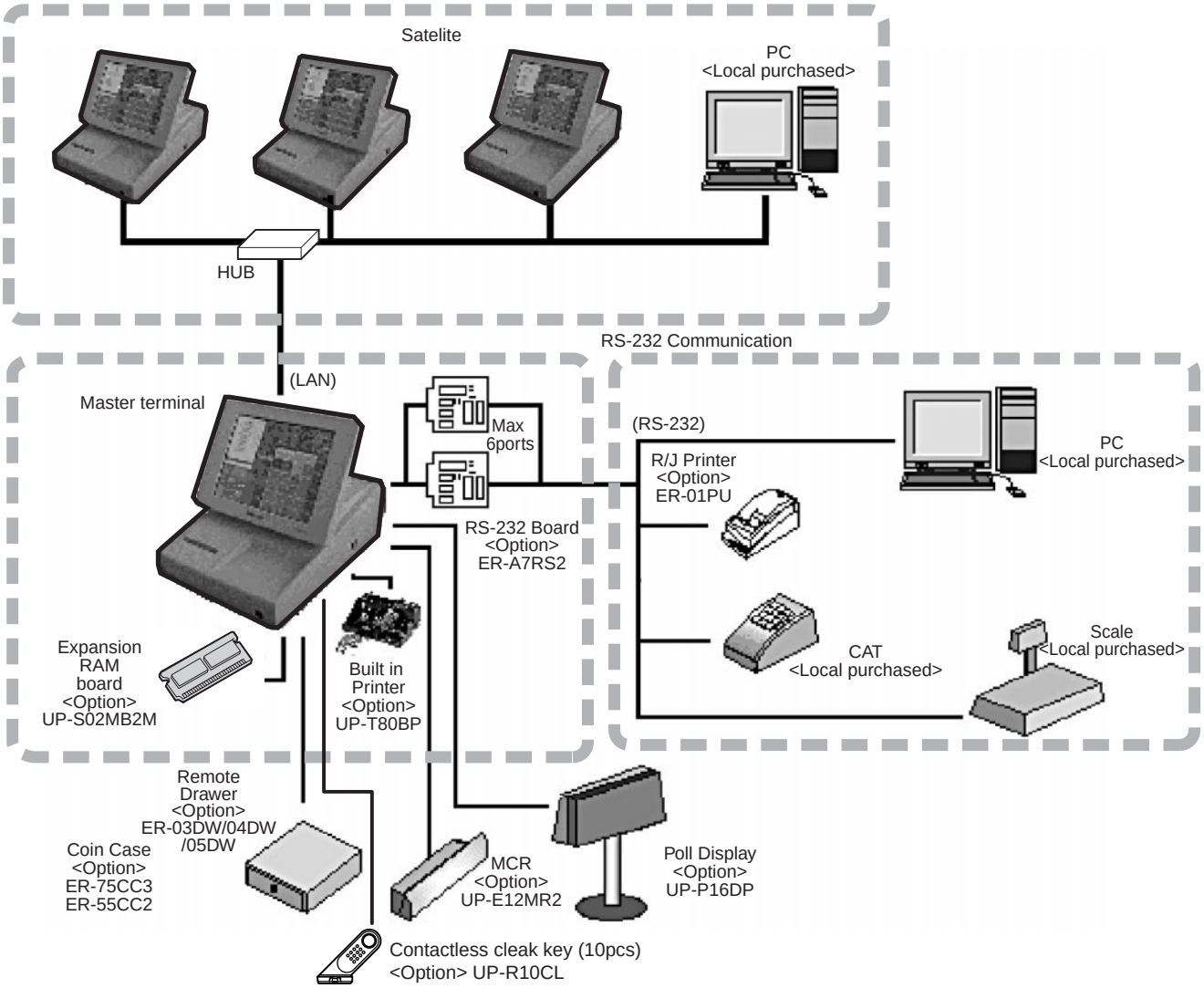
4) Display Adjustment

You can adjustment the brightness and contrast of the display by using the corresponding controls.


Brightness control
Turning the control backwards darkens the display and turning it forward brightens the display.
Contrast control
Turning the control backwards darkens the display and turning it forward lightens the display.

CHAPTER 2. OPTIONS

1. System configuration



2. Sales Options

No.	CLASSIFICATION	COMPONENT NAME	MODEL NAME	REMARK
1	Printer	External R/J printer	ER-01PU	Via RS-232 I/F
		Built-in printer	UP-T80BP	Via RS-232 I/F
2	Display	Remote display (Pole type)	UP-P16DP	11-Dig. 7-Seg. +16-Dig. Dot
		Customer display	UP-I16DP	11-Dig. 7-Seg. +16-Dig. Dot
3	Clerk	Contactless Clerk key	UP-R10CL	10pcs
4	Drawer	Remote drawer	ER-03DW	
			ER-04DW	
			ER-05DW	
		Coin case	ER-48CC2	4B/8C
			ER-48CC3	4B/8C
			ER-58CC	5B/8C
		Coin case cover	ER-01CV1-5	
			ER-02CV1-5	
			ER-03CV	
5	Memory	Expansion RAM disk board	UP-S02MB2M	2M bytes S-RAM board
6	On-line function	RS232 I/F board	ER-A7RS2	2 ports RS232 I/F
7	OTHER	MCR (Magnetic Card Reader)	UP-E12MR	for ISO 1 & 2 stripe card
		EFT terminal I/F	ER-02EF2	

3. Local purchase options

No.	COMPONENT NAME	MODEL NAME	NOTE
1	External printer	TM-T85/T88 (3)	Via RS-232 I/F
		TM-300/210/230	
2	Slip printer	TM-U295	

4. Service tools

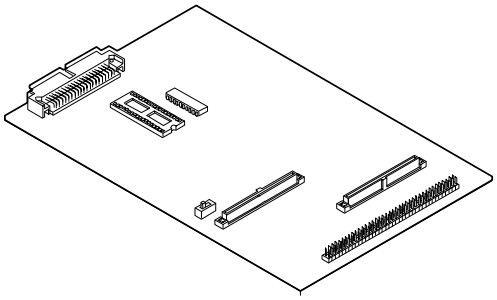
No.	NAME	PARTS CODE	PRICE	DESCRIPTION
1	MCR test card	UKOG-6718RCZZ	BE	for UP-E12MR2
2	RS232 loop back connector	UKOG-6705RCZZ	BC	for RS232 connector
3	Expansion PWB	CKOG-6724BHZZ	BQ	for ER-A7RS2

5. Supplies : None

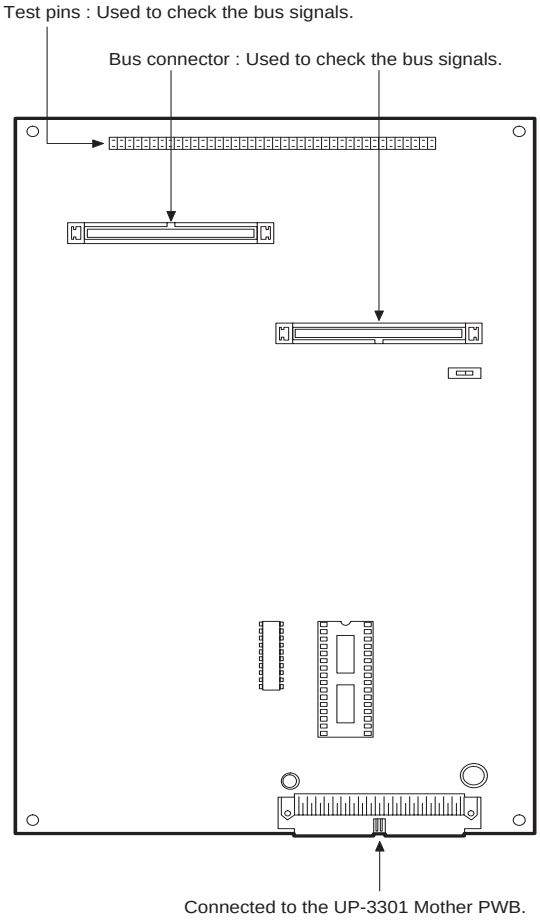
6. How to use the service tools

6-1. Expansion PWB : CKOG-6724BHZZ

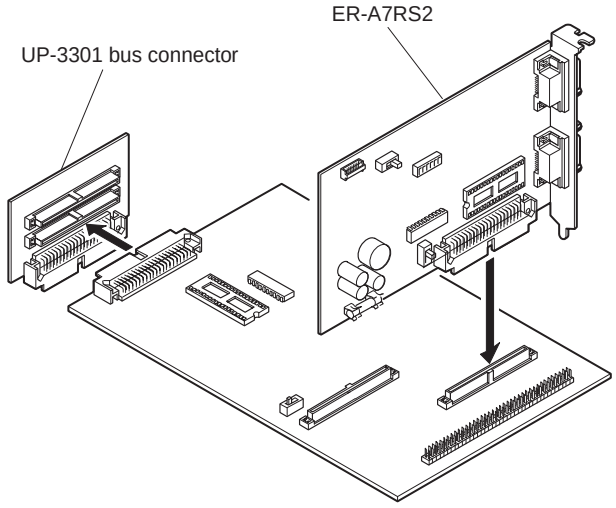
• Extrenal view



• Plain view



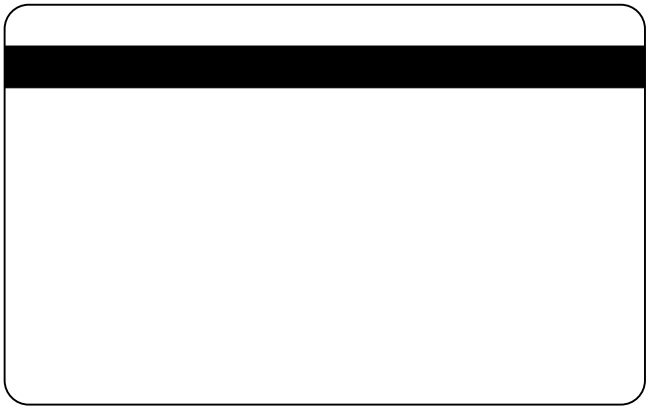
• Connection diagram



6-2. MCR test card: UKOG-6718RCZZ

• Used when executing the diagnostics for the UP-E12MR2.

• External view



CHAPTER 3. SERVICE PRECAUTION

1. Calibration

1. Calibration

The coordinates on the touch panel and those on the VGA display may not match for the following reasons.

- The physical deviation between the touch panel and LCD display
- Variations in “electric resistance>coordinate” conversion on the touch panel

Correction for such deviations is to perform the calibration.

2. Timing of starting calibration

Calibration is started in the following two cases:

– SRV reset/MRS –

1) When the touch panel is pressed:
   Calibration is started when a PROGRAM reset/MRS is performed with the touch panel pressed at the same time.
2) When no calibration has been performed:
   Calibration is started when the calibration data held by the touch panel controller is broken.

Note: Case 2 isn’t performed if case 1 is performed prior to the second.

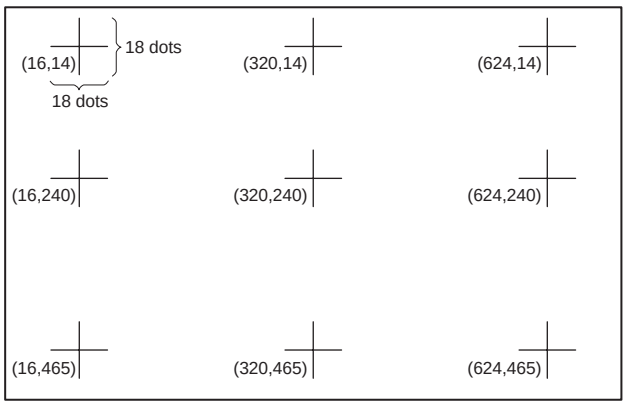
Calibration is also started when the EEPROM on the touch panel PWB is replaced.

Note: If the touch panel unit is replaced for any reason such as a repair, then start calibration, by following case 1).

3. Calibration specifications

1) The character text “Calibration Mode” is displayed.
2) If the touch panel is kept pressed, the machine waits for the finger leaving the touch panel.
3) The character text “Touch these crosses” is displayed.
4) Entering correction mode
   The command “Entering correction mode” is issued to the touch panel controller.
   At this step, the coordinate data of the four corners in the input area are passed to the controller.
5) Correction points are displayed
   The correction points are displayed.
   All of the nine correcting points are displayed as follows using the mark “+”. The “+” mark is 18 by 18 dots with 2 dots thick.

VGA Display



6) Correction points are input
   Arbitrary correction points are input. Coordinate data corresponding to its input are output from the touch controller. Note the data are those of the initial coordinates. (Refer to the table below.)
   The point from where the finger leaves the touch panel is defined as the correction point input position (OFF position).
   The data on the nearest correction point is checked, and if almost appropriate, (regarding data of the initial coordinates, within +/-100 dots and +/-5mm in size) the command “correction data set” is issued to the controller. When the panel is released and it is possible to correct the settings by touching the panel, changing the “+” mark green.
   If the input coordinates are very far from the correction point, it will be neglected. If the command “correction data set” is terminated normally, the mark “+” at the correction point turns black.
   The input coordinate data are those of the initial coordinates, and the relation to the correction points is as follows:

   The data of the initial coordinates of correction points

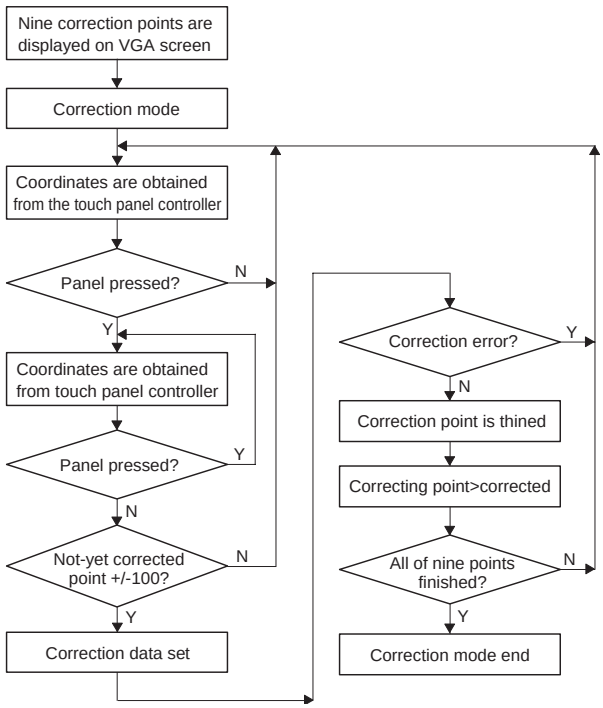
393, 402	2080, 402	3767, 402
393, 2048	2080, 2048	3767, 2048
393, 3697	2080, 3697	3767, 3697

7) Step 6) is repeated for the nine correction points.
   Correction is performed in an arbitrary order. At first all of the nine points are displayed in white and they turn black as corrected.
8) After all of the points are corrected, the command “correction mode end” is issued to the controller.
   The maximum coordinates are (4096, 4096).
9) The display mode is returned to the text mode.

∗If the power supply is turned off during correction, the following messages are displayed and all the steps are started over again.

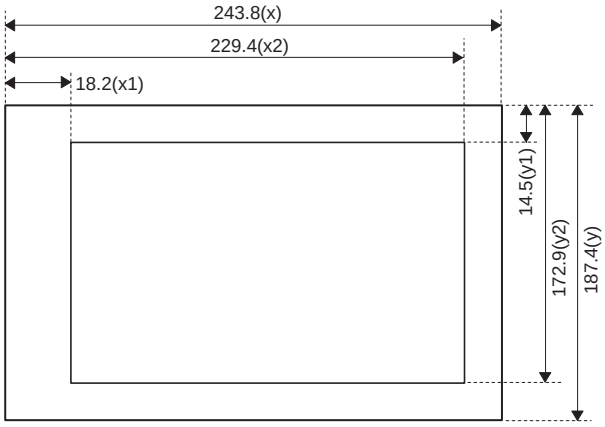
Calibration failed.
Touch the panel to try again

Calibration flow

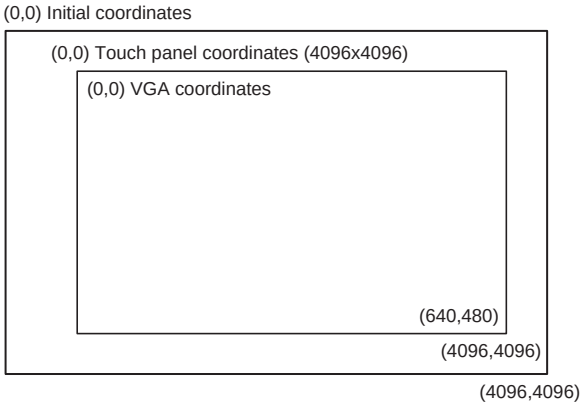


4. Touch panel/VGA coordinates

• Touch panel configuration (unit: mm)



• Touch panel coordinates



Initial coordinates (xi, yi) ↔ Touch panel coordinates (xt, yt) conversion

xt = (xi - 4096*x1/x)*(x / (x2-x1))
yt = (yi - 4096*y1/y)*(y / (y2-y1))

Touch panel coordinates (xt, yt) ↔ VGA coordinates (xv, yv) conversion

xv = xt * 640 / 4096
yv = yt * 480 / 4096

• Coordinates of correction points

Initial coordinates

393, 402	2080, 402	3767, 402
393, 2048	2080, 2048	3767, 2048
393, 3697	2080, 3697	3767, 3697

Touch panel coordinates

100, 100	2048, 100	3996, 100
100, 2048	2048, 2048	3996, 2048
100, 3996	2048, 3996	3996, 3996

VGA coordinates

16, 14	320, 14	624, 14
16, 240	320, 240	624, 240
16, 465	320, 465	624, 465

2. IPL (Initial Program Loading) function

1) Introduction

The application software of the UP-3301 is written in the flash ROM.

In the following cases, the writing procedure of the application software into the flash ROM is required

• When the flash ROM is replaced with a new one. The service part flash ROM does not include the application software in it.

• When IPL writing is required because of a change in the software.

∗The service part of the main PWB unit includes the flash ROM with the application software written in it. There is no need for writing the application software when replacing the main PWB unit.

2) IPL procedure

There are two ways of IPL procedures.

• IPL from EPROM via ER-A7RS2

• IPL from PC via the POSUTIL.EXE PC utility.

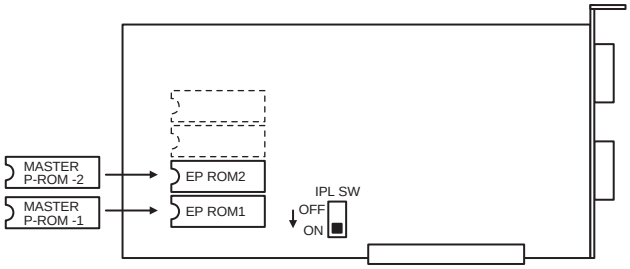
The detailed descriptions on the above procedures are given below.

3) IPL from P-ROM via ER-A7RS2

(1) Install the two master ROMs to the IC socket (IC12, IC13) on the ER-A7RS2.

Master ROM -1 : VHI27801RXXXX
Master ROM -2 : VHI27801RXXXX

(2) IPL switch on the ER-A7RS2 : Set the IPL SW to ON position.



(3) Install the ER-A7RS2 in the UP-3301. (The UP-3301 power should be turned OFF.)

(4) Turned on the power of the UP-3301.

(5) The IPL procedure is started.
After the buzzer sounds terminated, the IPL procedure finished.

(6) Turn OFF the power of the UP-3301.

(7) Remove the ER-A7RS2 from the UP-3301.

(8) Perform a Master reset.

3. POS UTILITY TOOLS

1) OUTLINE

This Specification document describes the explanation about "POSUTILITYTOOL.EXE and "02FD.EXE".

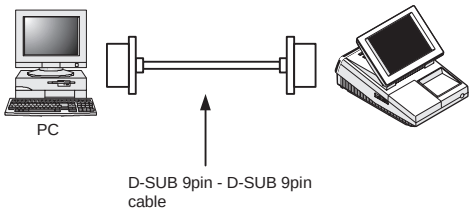
"POSUTILITYTOOL.EXE"and "02FD.EXE" works on Windows 95/98 of PC and they have the following
Functions by connecting UP-3301 with RS232.

POSUTILITYTOOL.EXE:	IPL of UP-3301 Program Object
02FD.EXE:	All RAM Data Upload/Download (PC software tool instead of the current ER-02FD.)

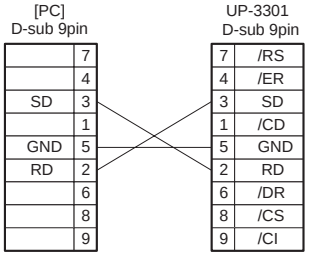
2) CONNECTION

PC and UP-3301 are connected by RS232.

Connect the CH2 port of the UP-3301 to the RS-232 interface of the PC.

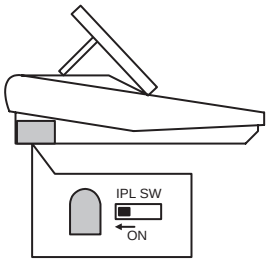
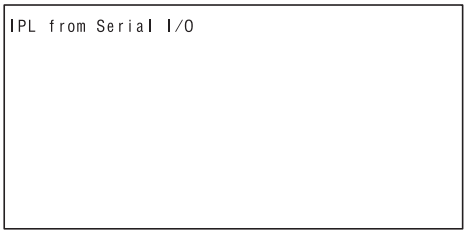


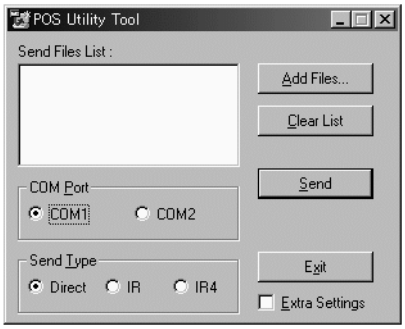
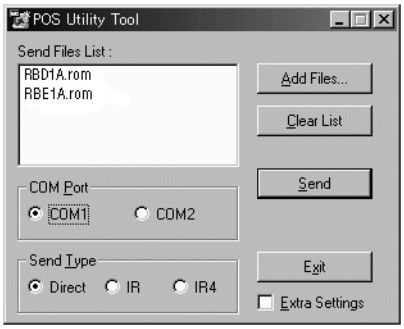
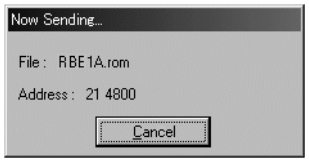
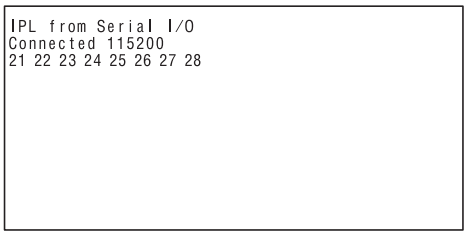
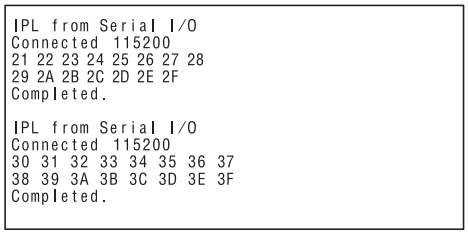
RS232 Cable Connecting:



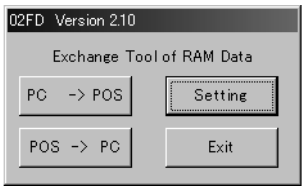
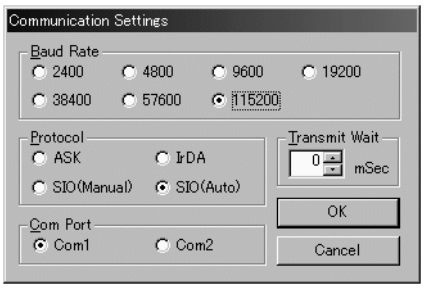
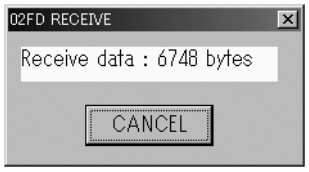
3) PROCEDURE

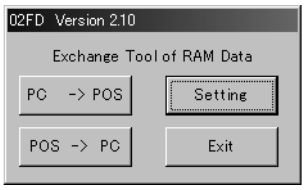
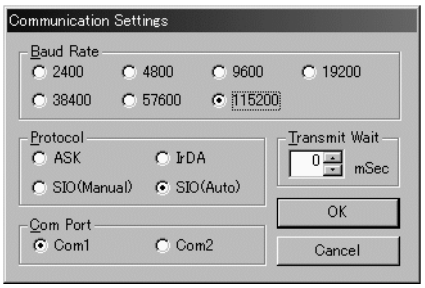
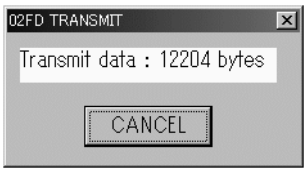
3) -1. POS UTILITY

No	Procedure on P.C. side	No	Procedure on UP-3301 side
1	Install the "POSUTILITYTOOL.EXE" on the P.C.		
		2	Turn OFF the power.
		3	Select "IPL Mode". Set the "IPL Switch" of the UP-3301 to "ON". 
		4	Turn ON the power.
		5	Starting of "IPL Mode". The UP-3301 displays "IPL from Serial I/O" 
6	Connect the P.C. and the UP-3301 (CH2) via RS232. (Fig 1)		

No	Procedure on P.C. side	No	Procedure on UP-3301 side
7	Execute the "POSUTILITUTOOL.EXE" on the P.C. *Please close all other applications while using this utility. 		
8	Select the ROM object Files by clicking the "Add Files.." button. 		
9	Push the "SEND" button. Program data is sent to the UP-3301 automatically. 	9	Program data is received from the P.C. automatically. The UP-3301 displays. 
10	When data sending is completed, the initial Window is shown after "Complete" window.	10	The UP-3301 displays "Completed." 
		11	Turn OFF the power.
		12	Select "Normal Mode". Set the "IPL switch" to "OFF".
		13	Execute the "Service Reset" on UP-3301.

3) -2. 02FD

No	Procedure on P.C. side	No	Procedure on UP-3301 side
1	Install the "02FD.EXE" on the P.C. ALL RAM Data UpLoad : Go to "2" ALL RAM Data DownLoad : Go to "9"		
2	ALL RAM Data UpLoad Connect the P.C. and the UP-3301 (CH2) via RS232.	2	Enter the SRV mode. Select " 2 SETTING ". Select " 13 DATA SEND"
		3	The UP-3301 displays DATA SEND SEND DATA ALL RAM SPEED PROGRAMMED SPEED
4	Execute the "02FD.EXE" on the P.C. *Please close all other applications while using this utility. 		
5	Set the Communication method by pushing the "Setting" Button.  Push the "OK" Button.		
6	Push the "[POS → PC]" Button. And Select the Receiving File.		
7	Communication starts. 	7	Push CASH key. The UP-3301 displays SENDING 00000
8	The UpLoad is completed. The initial Window is shown. Push the "Exit" Button.	8	The UpLoad is completed. The SETTING menu is shown.
9	ALL RAM Data UpLoad Connect the P.C. and the UP-3301 (CH2) via RS232.	9	Enter the SRV mode. Select " 2 SETTING". Select " 14 DATA RECEIVE"
		10	The UP-3301 displays BACKUP RECEIVE SPEED PROGRAMMED SPEED Push the CASH key.

No	Procedure on P.C. side	No	Procedure on UP-3301 side
11	Execute the "02FD.EXE" on the P.C. *Please close all other applications while using this utility. 		
12	Set the Communication method by pushing the "Setting" Button.  Push The "OK" Button.		
13	Push the "[POS → PC]" Button. And Select the Sending File.		
14	Communication starts. 	14	The UP-3301 displays
15	The DownLoad is completed. The initial Window is shown. Push the "Exit" Button.	15	The DownLoad is completed. The SETTING menu is shown.
		16	Execute the " Service Reset " on the UP-3301

4. UTL33.EXE (UP-3301 Series Utility tool)

1. Outline

This specification covers the utility program “UTL33.EXE” for UP-3301 series. The “UTL33.EXE” is a program which runs on the PC DOS prompt screen, it is connected to the UP-3301 by RS232 (CH2). It has the following functions: (1) UP-3301 IPL operation; (2) LOGO data rewrite for built-in printer UP- T80BP; and (3) program rewrite.

2. System requirements

PC and UP-3301 are connected by RS232 (CH2).

3. Functions

The following three functions become available:

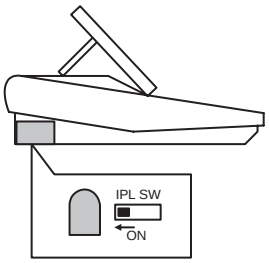
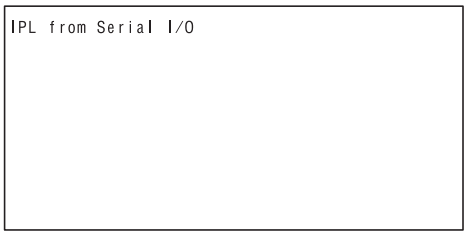
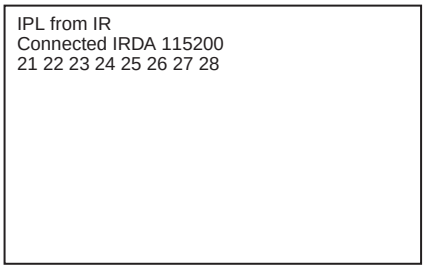
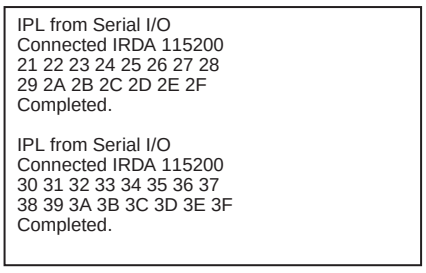
(1) UP-3301 program rewrite (IPL)
The UP-3301 program is updated. S-type files or ER01FD type data files are used for ROM data.

(2) LOGO data rewrite
The LOGO STAMP data for the UP-T80BP is set.
Black-and-white BMP/PCX data is used and the image size is up to 576 x 240 dots.

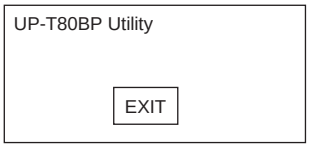
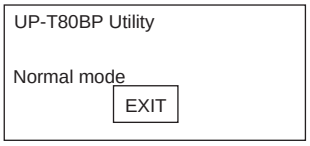
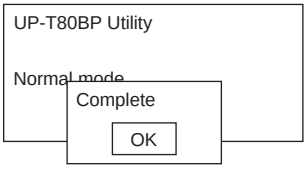
(3) Program rewrite (IPL)
The UP-T80BP program is updated. S-type files are used for ROM data.
According to the contents of the file, “UTL33.EXE” automatically selects the appropriate protocol from the three types described above. 1

4.

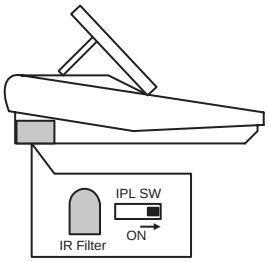
4.1 UP-3301 IPL

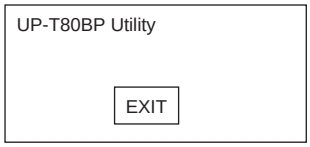
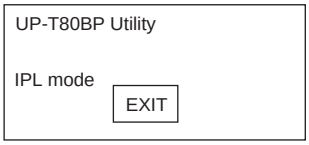
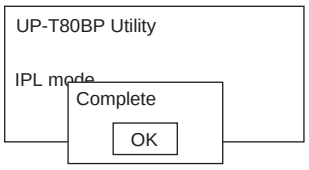
No	Procedure on P.C. side	No	Procedure on UP-3301 side
1	Install “UTL33.EXE” on the P.C.		
		2	Turn OFF the power.
		3	Select “IPL Mode”. Set the “IPL Switch” of UP-3301 to “ON”. 
		4	Turn ON the power.
		5	Starting of “IPL Mode”. The UP-3301 displays “IPL from Serial I/O” 
6	Connect P.C. and UP-3301 via RS232.		
7	Execute “UTL33.EXE” on P.C. Operation: **>UTL33 3301_1.ROM 3301_2.ROM** (“3301_1.ROM” and “3301_2.ROM” are file name of S-type ROM object.)		
8	Program data is sent to UP-3301 automatically.	8	Program data is received from P.C. automatically. The UP-3301 displays 
9	“UTL33.EXE” is completed. P.C. shows “Completed.”	9	The UP-3301 displays “Completed.” 
		10	Turn OFF the power.
		11	Select “Normal Mode”. Set the “IPL switch” to “OFF”.
		12	Execute the “Service Reset” on UP-3301.

4.2 UP-T80BP LOGO

No	Procedure on P.C. side	No	Procedure on UP-3301 side
1	Install “UTL33.EXE” on the P.C.		
		2	Enter the SRV mode. Then turn OFF the power or UP-3301.
		3	While pressing the On-Line key, tum ON the power of UP-3301. Keep pressing the On-Line key, and then press the Feed key also. (Don’t move a finger from the On-line key.)
		4	UP-T80BP enters into LOGO mode. UP-T80BP prints out “**********”.
		5	Go into “UP-T80BP Utility mode”. Select “6 UP-T80BP Utility” in SRV mode.
		6	Starting of “UP-T80BP Utility mode”. UP-3301 shows 
7	Connect P.C. and UP-3301 via RS232 (CH2).		
8	Execute “UTL33.EXE” on P.C. Operation: **>UTL33 LOGO.BMP** (“LOGO.BMP” is a file name of Bit-Map image.)		
9	Program data is sent to UP-3301 automatically.	9	Program data is received from P.C. automatically. 
10	“UTL33.EXE” is completed. P.C. shows “Completed.”	10	UP-3301 shows “Completed.”  And UP-T80BP prints out the LOGO image.
		11	Touch “OK” button.
		12	Touch “EXIT” button.
		13	Turn OFF the power of UP-3301.
		14	Execute “Master Reset” on UP-T80BP.

4.3 UP-T80BP IPL

No	Procedure on P.C. side	No	Procedure on UP-3301 side
1	Install “UTL33.EXE” on the P.C.		
		2	Turn OFF the power of UP-3301.
		3	Select “IPL Mode” on UP-T80BP. Set the Bit 1 of DipSwitch 2 to “ON” to enter “IPL Mode”. 
		4	While pressing both the Feed key and the On-Line key, turn ON the power of UP-3301. The ERROR Lamp and the On-line Lamp of UP-T80BP is blinking.

No	Procedure on P.C. side	No	Procedure on UP-3301 side
		5	UP-T80BP enters into IPL mode when the Feed key is pressed. (UP-T80BP clears the application program which is in its own flash ROM.) The ERROR Lamp is blinking and the On-Line Lamp is turned off.
		6	UP-T80BP waits the application program data. The ERROR Lamp is turned off and the On-Line Lamp is turned on.
		7	Enter “UP-T80BP Utility” mode. Select “6 UP-T80BP Utility” in SRV mode
		8	Starting of “UP-T80BP Utility” mode. UP-3301 shows 
9	Connect P.C. and UP-3301 via RS232 (CH2).		
10	Execute “UTL33.EXE” on P.C. Operation: **>UTL33 T80BP.ROM** (“T80BP.ROM” is a file name of S-type object.)		
11	Program data is sent to UP-3301 automatically.	11	Program data is received from P.C. automatically.  The On-line Lamp of UP-T80BP starts blinking.
12	“UTL33.EXE” is completed. P.C. shows “Completed.”	12	UP-3301 shows “Completed.”  The On-line Lamp of UP-T80BP stops blinking.
		13	Touch “OK” button.
		14	Touch “EXIT” button.
		15	Turn OFF the power of UP-3301.
		16	Select “Normal Mode” on UP-T80BP. Set the Bit 1 of DipSwitch 2 to “OFF” to enter “Nomal Mode”.
		17	Execute “Master Reset” on UP-T80BP.

<Usage of “UTL33.EXE”>

“UTL33.EXE” is a utility program on P.C. - a program that sends the application program data of UP-3301, the image data of the Logo stamp of UP-T80BP or the application program data of UP-T80BP in order to replace them.

Syntax

UTL33 [-Fn] [-Cn] filename [filename ...]

Parameter

filename

Specifies the name file which you want to send.

For UP-3301 IPL	S-type ROM object file
For UP-T80BP LOGO STAMP	BMP/PCX file
For UP-T80BP IPL	S-type ROM object file

Switches

-Fn

Specifies the function. Valid values for n are in the range 1 through 3.
1: UP-3301 IPL
2: UP-T80BP LOGO STAMP
3: UP-T80BP IPL
Normally, UTL33.EXE takes the suitable function automatically.
If the automatic selection does not work correctly, please use this switch.

-Cn

Specifies the number of the serial (COM) port. Valid values for n are in the range 1 through 2.
The default value is 1 (COM1).

Example

For UP-3301 IPL.

UTL33 3301_1.ROM 3301_2.ROM

For UP-T80BP LOGO STAMP (To use COM2).

UTL33 -C2 LOGO.BMP

For UP-T80BP IPL (To use the switch “-F”).

UTL33 -F3 80BP.ROM.

5. Requirements for soldering circuit parts

To solder the following parts manually, follow the conditions described below.

PARTS NAME	PARTS CODE	LOCATION	CONDITIONS FOR SOLDERING
Ceramic oscillator	RCRMZ7002RCZZ	MAIN PWB: X1 (8M)	270°/3sec.
	RCRMZ7004RCZZ	MAIN PWB: X2 (7.37M)	270°/3sec.

6. Note for handling of Touch panel

- The transparency of the touch panel is vitally important. Do not place finger prints or moisture on the surface. When handling, use clean gloves and masks.
- For handling, do not hold the transparent area, and do not hold the heat seal connector section to assure reliability.
- Do not overlay touch panels. The edge may damage the surface.
- Do not put a heavy object on the touch panel.
- Do not apply strong shocks, and do not drop.
- When attaching the protection film, carefully check that no dirt exists.
- To clean dirt on the surface, use a dry, soft cloth or a cloth immersed in ethyl alcohol.
- Check that the housing does not induce any stress to the touch panel.
- Be careful not to touch the touch panel with tools.
- The heat seal section is easily disconnected. Be careful not to apply any stress to the heat seal section when installing.
- The touch panel is provided with an air groove to make the external and the internal air pressure equal to each other. If water or oil is put around the air groove, it may penetrate inside. Be careful and keep the air groove away from water and oil.
- Input is performed with fingers. Do not use hard objects to input entries.

7. Note for handling the LCD assembly

- The LCD elements are made of glass. BE careful not to expose them to a strong mechanical shock. Use extreme care not to break them.
- If the LCD element is broken and the liquid is seeps, do not lick it. If the liquid comes in contact with your skin or clothes, immediately clean with soap.
- Use the unit under the rated conditions to prevent against damage.
- Be careful not to drop water or other liquids on the display surface.
- The reflection plate and the polarizing plate can be easily scratched. Be careful not to touch them with any hard object such as glass or tweezers. Never hit, push, or rub the surface with hard objects.
- When installing the unit, be careful not to apply stress to the LCD module. If excessive stress is applied an abnormal display or uneven color may result.

8. Cautions on handling connectors

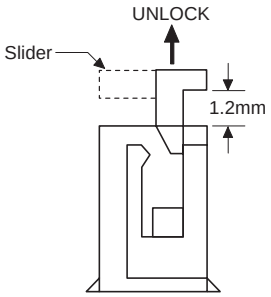
When connecting or disconnecting the following connectors, follow the procedures below.

1)

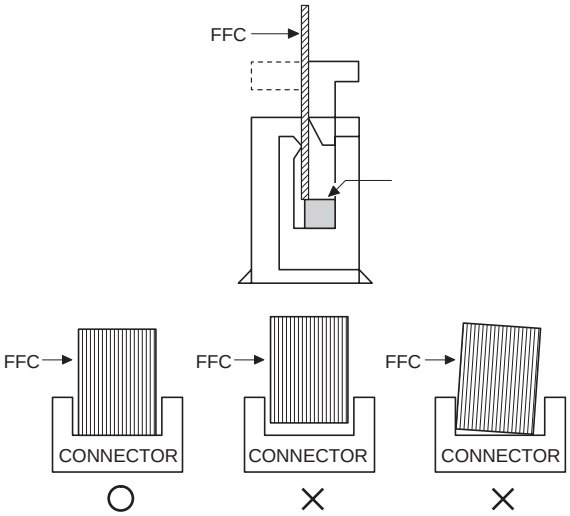
PARTS NAME	PARTS CODE	LOCATION
FFC CONNECTOR	QCNCW7207RC4J	MAIN PWB: CN6 TOUCH PWB: CN5
FFC CONNECTOR	QCNCW7183BH2F	MAIN PWB: CN1

• How to Connect or Disconnect the FFC Connector

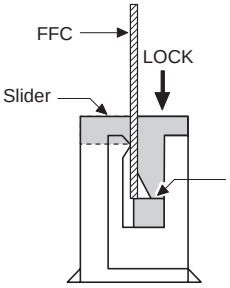
(1) Open the slider to the unlock position
The slider will open only up to a fixed height (about 1.2mm). If you used force to pull up the slider further, it may be damaged.



(2) Insert the FFC
Insert the FFC firmly untill the FFC hits the bottom of the connector's insulator.



(3) Close the slider to the lock position
Insert the FFC and then push the slider downward.

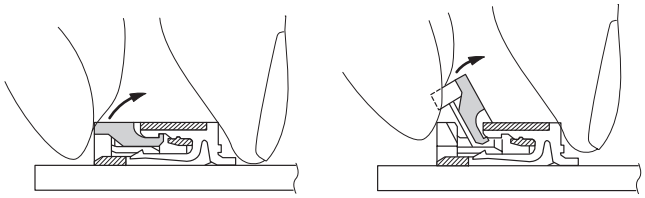


2)

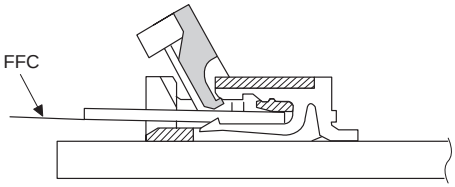
PARTS NAME	PARTS CODE	LOCATION
FFC CONNECTOR	QCNCW7217RC3J	TOUCH PWB: CN1

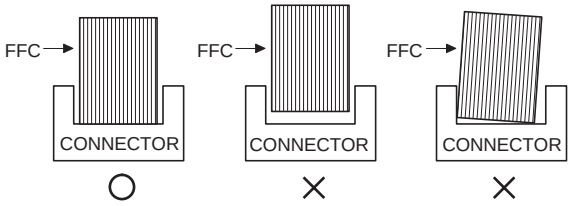
• How to Insert the FFC Connector

(1) Open the slider to the unlock position
Open the slider upwards up to an angle of 60 degrees. If the slider does not fully open, the FFC can not be smoothly inserted.

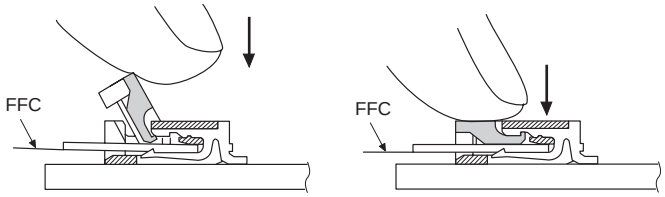


(2) Insert the FFC
Insert the FFC firmly until the FFC hits the bottom of the connector's insulator.





(3) Close the slider to the lock position
Insert the FFC and then push the slider downward.



(4) To pull out the FFC out, unlock the slider, then pull it out in the same procedures as (1).

9. Caution for handling the Rear Display PWB unit

SYSTEM RESET is controlled by the battery-protected CKDC9 (1 chip microcomputer) on the rear display PWB.

CHAPTER 4. PROGRAM RESET AND SRV MODE

In the UP-3301, the following reset switch (location No: S1) is used to switch to the service (SRV) mode and to reset.

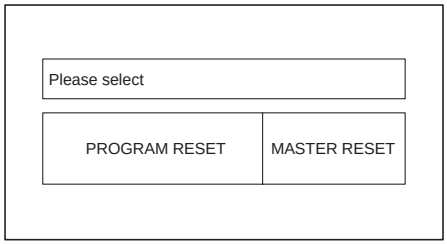
PROGRAM RESET

Used to return the machine back to its operation state after a lock up has occured.

PROCEDURE

1) Turn off the AC power switch.
2) Set the reset switch to the "ON" position.
3) Turn on the AC power switch.
4) Set the reset switch to the "OFF" position.
5) The reset menu window is displayed as shown below.

DISPLAY:

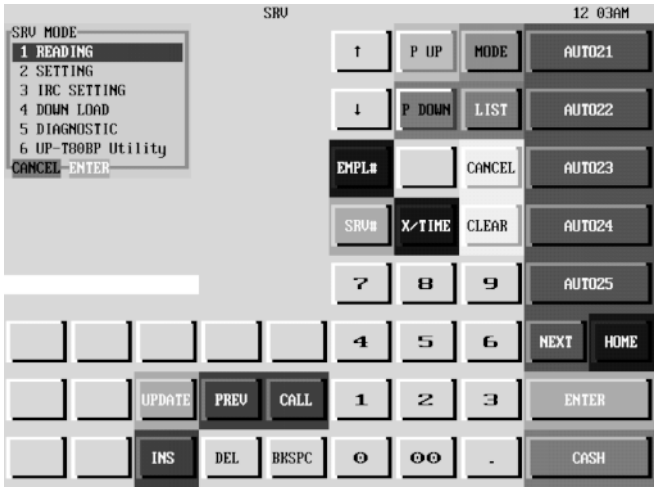


Touch the [PROGRAM RESET] key.

6) PROGRAM RESET is executed.
7) After completion of the program reset, the SRV mode is displayed as shown below.

DISPLAY:

[SRV mode screen]



CHAPTER 5. MASTER RESET (ALL MEMORY CLEAR)

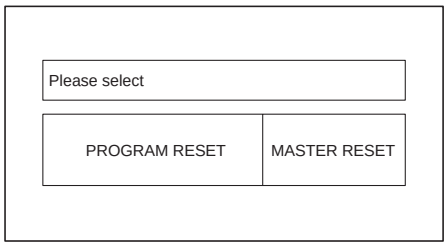
There are three possible methods to perform a master reset.

1. MRS-1 (Master Reset-1): Clear the entire memory and resume initial values.

PROCEDURE

1) Turn off the AC power switch.
2) Set the reset switch to the "ON" position.
3) Turn on the AC power switch.
4) Set the reset switch to the "OFF" position.
5) The reset menu window is displayed as shown below.

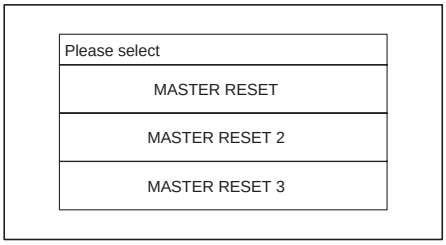
   DISPLAY:



   Touch the [MASTER RESET] key.

6) The master reset menu window is displayed as shown below.

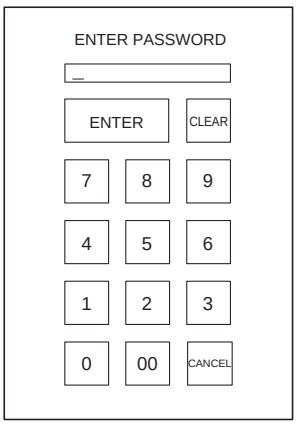
   DISPLAY:



   Touch the [MASTER RESET] key.

7) The secret number entry window is displayed as shown below.

   DISPLAY:



   Enter the secret number for the MASTER RESET-1 and touch the [ENTER] key.
   The secret number for MRS-1: 11111111

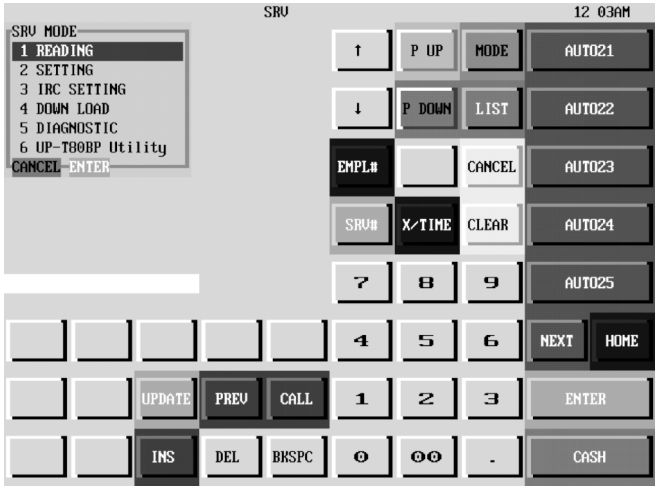
8) MASTER RESET-1 is executed.

   DISPLAY:

9) After completion of the master reset, the buzzer sounds three times and the following SRV mode display is shown.

   DISPLAY:

   [SRV mode screen]



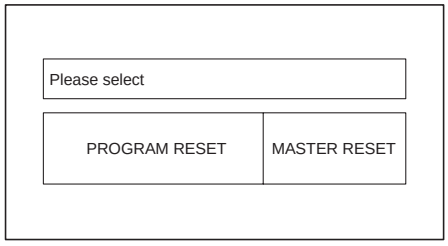
2. MRS-2 (Master Reset-2): Clear the entire memory and resumes initial values.

The keyboard must be entered by hand. This reset is used if an application needs different keyboard layout other than that supplied by a normal MRS-1.

PROCEDURE

1) Turn off the AC power switch.
2) Set the reset switch to "ON" position.
3) Turn on the AC power switch.
4) Set the reset switch to the "OFF" position.
5) The reset menu window is displayed as shown below.

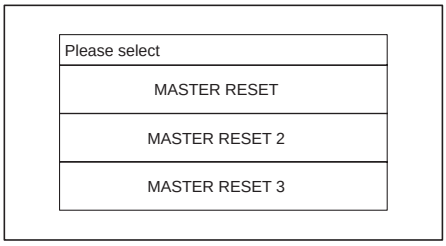
DISPLAY:



Touch the [MASTER RESET] key.

6) The master reset menu window is displayed as shown below.

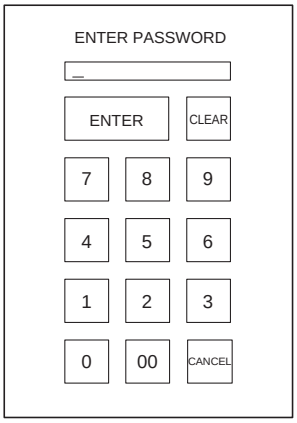
DISPLAY:



Touch the [MASTER RESET 2] key.

7) The secret number entry window is displayed as shown below.

DISPLAY:



Enter the secret number for the MASTER RESET-2 and touch the [ENTER] key.
The secret number for MRS-2: 22222222

8) Set the fixed keys in the table below (Start from the [HOME] key, The keys are displayed sequentially)

DISPLAY:

No.	KEY NAME
1	HOME
2	CANCEL
3	CL
4	MODE
5	UP (↑)
6	DOWN (↓)

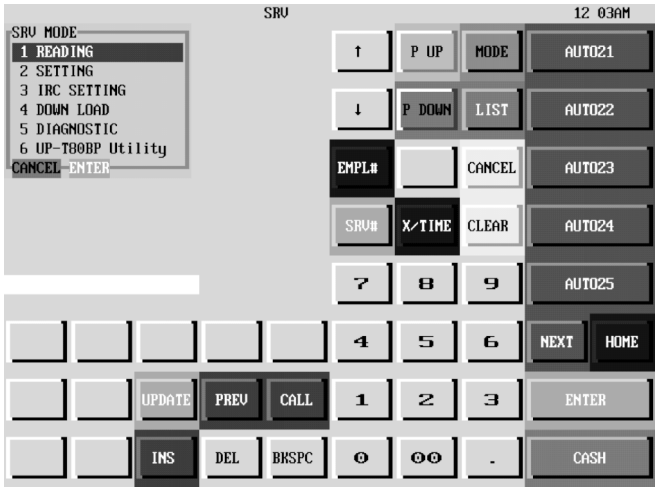
9) The MASTER RESET-2 is executed.

DISPLAY:

10) After completion of the master reset, the buzzer sounds three times and the following SRV mode display is shown.

DISPLAY:

[SRV mode screen]



3. MRS-3 (Master Reset-3): The Master reset 3 operation requires the entry of Serial No. in addition to master resetting 1.

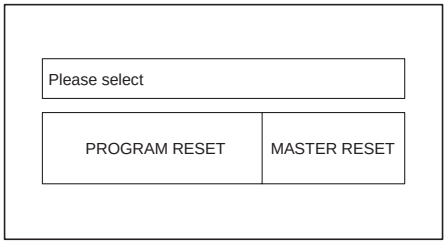
After completion of a MRS3, the following operations and programming will be inhibited.

1. GT programming.
2. GT resets with the transaction Z report. (Z report can be made, but GT will not be reset.)

PROCEDURE

1) Turn off the AC power switch.
2) Set the reset switch to the "ON" position.
3) Turn on the AC power switch.
4) Set the reset switch to the "OFF" position.
5) The reset menu window is displayed as shown below.

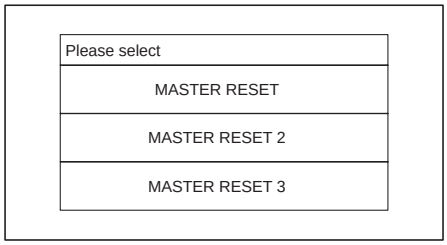
DISPLAY:



Touch the [MASTER RESET] key.

6) The master reset menu window is displayed as shown below.

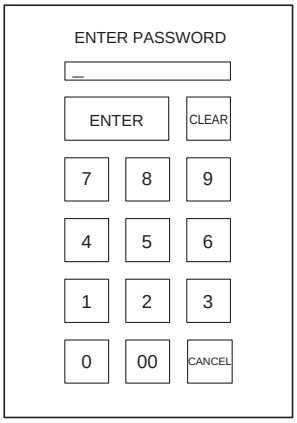
DISPLAY:



Touch the [MASTER RESET 3] key.

7) The secret number entry window is displayed as shown below.

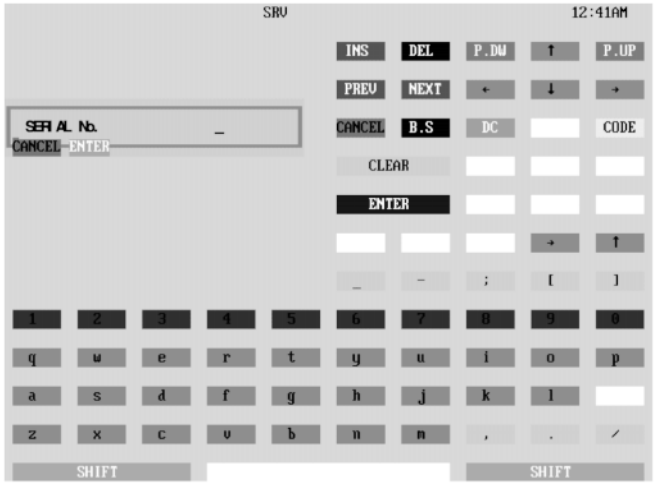
DISPLAY:



Enter the secret number for the MASTER RESET-3 and touch the [ENTER] key.
The secret number for MRS-3: 33333333

8) The product serial No. input window is displayed as shown below.

DISPLAY:



Enter the serial No. of the POS and touch the [ENTER] key.

9) Set the fixed keys in the table below (Start from the [HOME] key, The keys are displayed sequentially)

DISPLAY:

No.	KEY NAME
1	HOME
2	CANCEL
3	CL
4	MODE
5	UP (↑)
6	DOWN (↓)

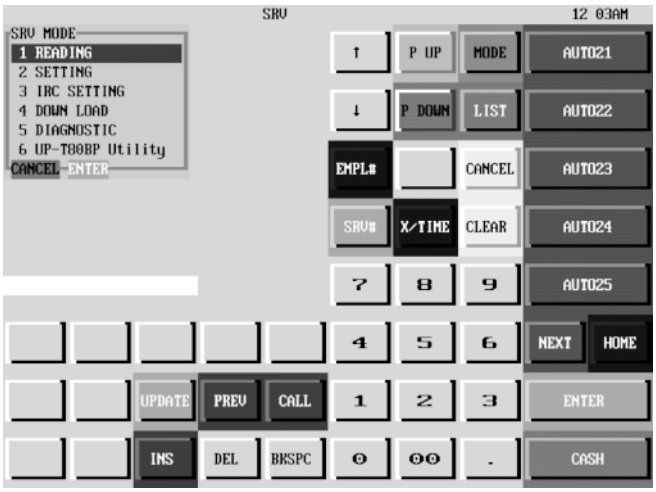
10) MASTER RESET-3 is executed.

DISPLAY:

11) After the completion of the master reset, the buzzer sounds three times and the following SRV mode display is shown.

DISPLAY:

[SRV mode screen]



CHAPTER 6. DIAGNOSTICS SPECIFICATIONS

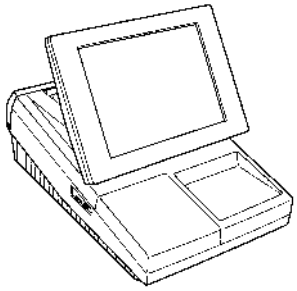
1. General

This diagnostics program is used for a simplified check of the UP-3301 series operations in servicing.
The diagnostics program is built in the standard ROM.

2. System configuration

2-1. Test system

UP-3301 only



3. Diagnostics

Starting the diagnostics

This diagnostics program is written in the external ROM and executed by the CPU (H8/510). To operate this program, the following conditions must be satisfied.

① The power for the logic system is proper. (+5V, VCKDC, POFF, +20V)

② The input/output pins and the internal logic of the CPU are normal. In addition, CKDC9, MPCA8, the system bus, and the standard ROM/RAM are normal.

Note: When booting the set for the first time, carry out the TOUCH KEY CALIBRATION and MASTER RESETTING.
In order to add an option unit when the machine is normally operating, perform the PROGRAM RESETTING.

1) Master reset procedure

① Turn off the AC power switch.

② Set the CKDC reset switch to the RESET position.

③ Turn on the AC power switch.

④ While touching the touch panel, place the CKDC RESET SWITCH to the normal position.

⑤ Perform CALIBRATION.

⑥ Select the MASTER RESET from the menu and execute it.

1) Standard RAM Check

① Check content

2) Program reset (service reset) procedure

① Turn off the AC power switch.

② Set the CKDC reset switch to the RESET position.

③ Turn on the AC power switch.

④ Set the CKDC reset switch to the normal position. (Do not press the touch panel.)

⑤ Select PROGRAM RESET from the menu and execute.

3-1. Execution of diagnostics

To start the diagnostics, select "DIAGNOSTICS" from the menu selection in SRV mode.

The DIAG MAIN MENU is started and the following menu screen is displayed. The selected individual diagnostics program is executed. When the individual diagnostics program is completed, the display returns to the menu screen. To terminate the diagnostics, press the CANCEL key. Then the display returns to the SRV mode menu screen.

UP-3301 Diagnostics V1.0A

Product & Test Diag	Drawer Diag
RAM Diag	Rear Display Diag
ROM & SSP Diag	MCR Diag
Clock Diag	Printer Diag
Touch Panel Diag	EFT Diag
Serial I/O Diag	
LCD Diag	Contactless Clerk Diag
TCP/IP Diag	Cancel

WARNING: "Product & Test Diagnostics" is used only in the production process, and must not be used in servicing.

3-2. RAM Diagnostics

This diagnostics is intended to test the standard and the extended RAM.

When you select RAM Diag, the following menu screen is displayed. Touch the key of the diagnostic you want to execute. Touch Cancel key to return to the Diag Main menu.

RAM Diagnostics

Standard RAM Check	
UP-S02MB2M Check	
	Cancel

For the SRAM of the standard 2MB RAM, the following test is performed. The memory contents will not be changed by this check.

The following processes are performed for the memory address (600000H~7FFFFFH) to be checked.

PASS1: Memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read/compare, data "5555H" write

PASS4: Data "5555H" read/compare, data "AAAAH" write

PASS5: Data "AAAAH" read/compare

PASS6: Memory data writed the saved data

In case of a compare error in the check sequences of PASS1~PASS6, an error display is displayed. If there is no error at all, the check is terminated normally.

In addition, the following address check is performed.

In case of an error, an error is made and read/write of the address where the error occurred is repeated.

Check point address = 600000H, 600001H
600002H, 600004H
600008H, 600010H
600020H, 600040H
600080H, 600100H
600200H, 600400H
600800H, 601000H
602000H, 604000H
608000H, 610000H
620000H, 640000H
680000H, 700000H

② Display

```
Standard RAM Check

   Standard memory size: 2048KB PASS!! (or ERROR!!)

   Error Address  xxxxxxH
      Write Data     xxxxH
      Read Data      xxxxH
```

The error address and the bit are displayed only when an error occurs. (If the error does not occur, the error address will not be displayed.)

③ Terminating procedure

After completion of the test, press the Touch panel.

2) UP-S02MB2 Check

① Check content

The UP-S02MB2 presence check is performed in the following procedure. The memory contents will not be changed by this check.

- 55AAH is written into 9FFFFEH.
- 9FFFFEH is read at the time of the synchronous command of E clock and compared with 55AAH. If both data are correct, the following procedure is performed. If not, "Extended RAM size: 0KB" is displayed and the test is terminated.

The following processes are performed for the check address (800000H~9FFFFFH).

PASS1: Memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read/compare, data "5555H" write

PASS4: Data "5555H" read/compare, data "AAAAH" write

PASS5: Data "AAAAH" read/compare

PASS6: Memory data writes the saved data

In case of a compare error in the check sequences of PASS1 ~ PASS6, an error display is made. If there is no error at all, the check is normally terminated.

In addition, the following address check is performed in the above test sequence.

In case of an error, an error display is made and the read/write address of the where the error occurred is repeated.

If there is no error at all check point address, "Extended RAM size: 2048KB PASS!!" is displayed and the test is terminated.

Check point address = 800000H, 800001H
800002H, 800004H
800008H, 800010H
800020H, 800040H
800080H, 800100H
800200H, 800400H
800800H, 801000H
802000H, 804000H
808000H, 810000H
820000H, 840000H
880000H, 900000H

② Display

```
UP-S02MB2 Check

   Extended RAM size : 2048KB       PASS!!(or ERROR!!)

   ErrorAddress   xxxxxxH
      WriteData      xxxxH
      ReadData       xxxxH
```

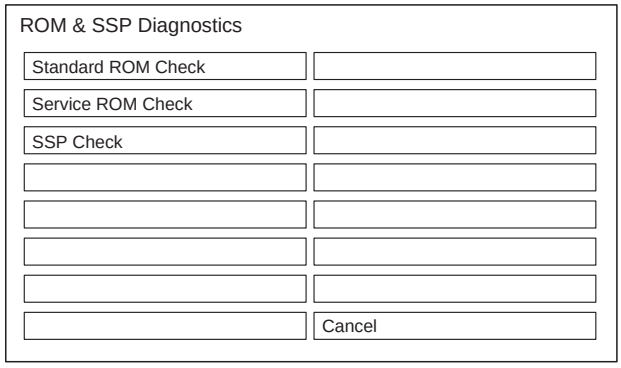
The error address and the bit are displayed only when the error occurs. (If the error does not occur, the error address will not be displayed.)

③ Terminating procedure

After completion of the test, press the Touch panel.

3-3. ROM & SSP Diagnostics

The standard ROM and the service ROM are checked. The SSP circuit is also checked.
The following menu is displayed. Press the desired key for of the operation you want to execute to execute individual Diag programs.
Pressing the CANCEL key returns the screen to the Diag MAIN menu.



1) Standard ROM Check

① Details of checking

Perform the following checks on each 1Mbyte in the standard ROM area (200000H - 5FFFFFH).
For the area "200000H - 2FFFFFH", read the character string stored in the address "21FFF0H - 21FFF5H". If it reads "27801R" or "sample", add the area "200000H - 2FFFFFH" to the byte unit. If the lower 2 digits are 10H as a result of the addition, the area is regarded as normal. Perform the same check on the areas after 300000H. If the lower 2 digits are not 10H as a result of the addition, the error message is displayed. If the character string is not "27801R" or "sample", it is regarded that any program is not stored in the areas after that area and the sum check is terminated.
For the area "300000H - 3FFFFFH", read the character string stored in the address "31FFF0H - 31FFF5H". If it reads "27801R" or "sample", add the area "300000H - 3FFFFFH" to the byte unit to check whether it is normal or not.
Perform the same check on the areas "400000H - 4FFFFFH" and "500000H - 5FFFFFH".
If there is no errors when the sum check is finished, the message "Standard ROM Sum Check: PASS!!" appears.
The ROM version and model code stored in the address "21FFE0H - 31FFFFH" are also displayed.
The formats of data (ASCII) stored are as follows:

21FFE0H - 21FFEFH:	MODEL CODE (e.g. UP-3301". Displayed until data becomes 00H.)
21FFF0H - 21FFF9H:	27801R **** (**** = Program version)
21FFFAH - 21FFFBH:	BLOCK NO. ("20" - "5F")
21FFFCH:	TERMINATOR ("=")
21FFFDH - 21FFFEH:	BLOCK VERSION (e.g. "00")
21FFFFH:	CHECK SUM CORRECTION DATA

The Flash ROM, used as the standard ROM, has 64-Kbyte unit rewrite blocks. To control the version in blocks, it is organized in the same 16-byte configuration as those after the aforementioned 21FFF0H and arranged for each 64 Kbyte. At this time, the sum of each block is corrected to become 01H and thus the sum of the entire 1 Mbyte becomes 10H.
The master EPROM (8 Mbits) for writing Flash ROM consists of 4 chips. To make it possible to control the program version by the chip, the program version stored in the blocks 21H, 31H, 41H and 51H are displayed. If the beginning of each ROM version stored in the blocks 21H, 31H, 41H and 51H is not "27801R" or "sample", it is regarded that the area does not have any program stored, and thus no program version is displayed.
In addition, the 0 PAGE (Block) where IPL is stored shows the program version of IPL so that it can control programs individually.

② Display

```
Standard ROM Check

  Standard ROM Sum Check : PASS!! (or ERROR!!)

  IPL PROGRAM Version
                **

  APL PROGRAM Version
          27801R****  UP-3301   ←Display the version.
          27801R****  UP-3301
          27801R****  UP-3301
          27801R****  UP-3301

  BLOCK   Version
    20=** 21=** 22=** 23=** 24=** 25=** 26=** 27=**
    28=** 29=** 2A=** 2B=** 2C=** 2D=** 2E=** 2F=**
                                :
                                :
```

③ Terminating procedure

After completion of the test, press the Touch panel.

2) SERVICE ROM Check

① Check content

The service ROM (EPROM × 4 Chip) area (D00000H - EFFFFFH) (supported by BANK switching) is added in the unit of byte. If the lower two digits of the result is 10H, it is normal. If the beginning of each ROM version stored in the each chip is not "27801R" or "sample", it is regarded that the area does not have any EPROM stored, and the sum check is not performed. The ROM version and the model name code which are stored in address D1FFE0H - D1FFFFH where the ROM version and the check sum correction data are stored is displayed. If the beginning of each ROM version stored in the each chip is not "27801R" or "sample", it is regarded that the area does not have any EPROM stored, and thus no program version is displayed. The format of data (ASCII) to be stored is as follows:

D1FFE0H - D1FFEFH:	Model name code (example: UP-3301. Display is made up to 00H of data.)
D1FFF0H - D1FFF9H:	27801R**** (**** = PROGRAM VERSION)
D1FFFAH - D1FFFBH:	BLOCK NO. ("20" - "5F")
D1FFFCH:	TERMINATOR ("=")
D1FFFDH - D1FFFEH:	BLOCK VERSION (example "00")
D1FFFFH:	CHECK SUM CORRECTION DATA

This SERVICE ROM allows to write into the FLASH ROM when re-execution is impossible because of an abnormality during rewriting into the FLASH ROM. The composition is the same as the standard ROM.

The program version of the IPL is displayed so that the 0 PAGE where the IPL is stored is individually controlled.

② Display

```
Service ROM Check

    Service ROM Sum Check 1 : PASS!!(or ERROR!!)
    Service ROM Sum Check 2 : PASS!!(or ERROR!!)
    Service ROM Sum Check 3 : PASS!!(or ERROR!!)
    Service ROM Sum Check 4 : PASS!!(or ERROR!!)

    IPL PROGRAM Version
                    **    ←Display the version

    APL PROGRAM Version
            27801R****  UP-3301
            27801R****  UP-3301
            27801R****  UP-3301
            27801R****  UP-3301

    BLOCK   Version
       20=** 21=** 22=** 23=** 24=** 25=** 26=** 27=**
       28=** 29=** 2A=** 2B=** 2C=** 2D=** 2E=** 2F=**
                              :
                              :
```

③ Terminating procedure

After completion of the test, press the Touch panel.

3) SSP Check

① Check content

By starting this diagnostic program, the SSP setting for testing is automatically performed and the SSP check is executed and the result is displayed.

The SSP check sets data for checking in the vacant space of the SSP entry register, and deletes the data that is checked after completion of the test. Therefore, existing data is not changed by this check.

② Display

```
SSP Check

    SSP (NMI) Check              : PASS!! (ERROR!!)
```

③ Terminating procedure

After completion of the test, press the Touch panel.

3-4. Clock & Clerk Switch Diagnostics

The operation of the clock crystal of the CKDC and the clerk switch are tested.

1) Timer & Clerk SW Check

① Check content

The operation of the CKDC9 clock crystal is checked.

The indication "YY/MM/DD & MM:HH:SS" is continuously updated. Check the time updated and indicated.

The code of the key inserted in the clerk key switch is displayed with hexadecimal.

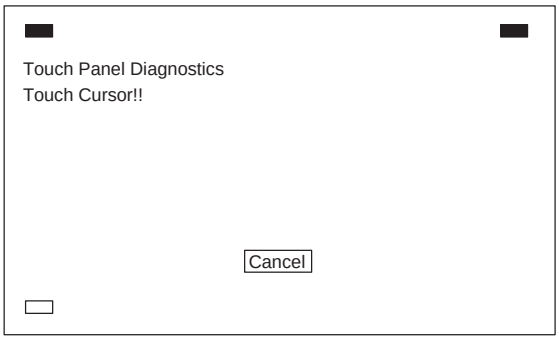
```
Timer & Clerk SW Diagnostics

    DATE&TIMER = YY/MM/DD &HH:MM:SS
    CLERK CODE = ***
```

3-5. Touch Panel Diagnostics

1) Touch Panel Check

① Check content

The input test of the touch panel is as follows: a rectangle of dotted lines is displayed at the corner of the LCD screen in the order of upper right, upper left, lower left, and lower right. Check whether a catch sound is heard and the rectangle turns black when each position is touched.



② End

The test is over when the four corners have been touched. To exit, please press the cancel key.

3-6. RS232 I/F Diagnostics

The main PWB and the optional PWB (RS232 interface of ER-A7RS2) are checked. Attach the 9-pin D-Sub loop back connector (UKOG-6717RCZZ). The wiring diagram is shown below (Fig. 6-1).

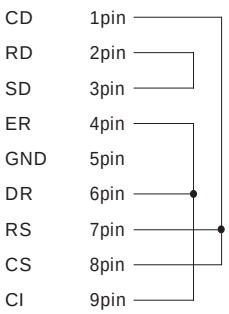
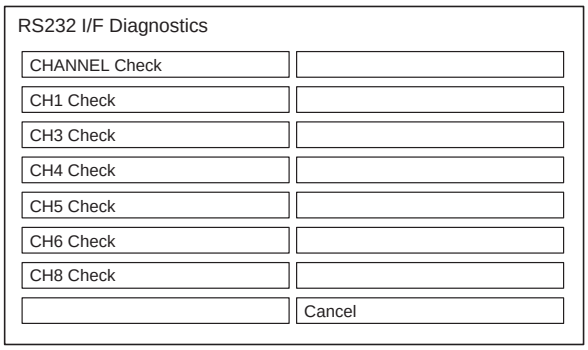


Fig. 6-1.

The following menu is displayed. Press the desired key for the operation you want to execute for the individual diagnostics programs.

Pressing the CANCEL key returns the screen to the Diag MAIN menu.

IMPORTANT : When setting channels for the RS232, do not set two or more ports to one channel. In the UP-3301, a max. two units of ER-A7RS2 can be installed. On each PWB, do not set two or more ports to the same channel. If two or more ports should be set to the same channel, the hardware can be damaged.



1) CHANNEL Check

① Check content

The CHANNEL setting of the connected RS232 is displayed. The display content and the setting of the DIP SW for CHANNEL setting on the RS232 I/F PWB are compared.

Since the RS232, printer port and port for noncontact setting on the main PWB of the UP-3301 is fixed to CH1, CH2, CH7 and CH8. The ER-A7RS2 must be set to CH3~CH6.

```
RS232 I/F Diagnostic

   CHANNEL Check
   CH1 = exist!      ←Display when the channel exists
   CH2 = exist!
   CH3 = none!       ←Display when the channel doesn't exist
   CH4 = none!
   CH5 = none!
   CH6 = none!
   CH7 = exist!
   CH8 = exist!
```

(Reference) ER-A7RS2 CHANNEL setting (In the table below, "1" = SW OFF, "0" = SW ON.)

ER-A7RS2 CON3

S1-1	S1-2	S1-3	CHANNEL
0	0	0	Invalid
0	0	1	CHANNEL 1: Do not set this (Reserved for standard RS)
0	1	0	CHANNEL 2: Do not set this (Reserved for noncontact clerk setting)
0	1	1	CHANNEL 3
1	0	0	CHANNEL 4
1	0	1	CHANNEL 5
1	1	0	CHANNEL 6:
1	1	1	CHANNEL 7: Do not set this (Reserved for internal printer)

ER-A7RS2 CON4

S1-4	S1-5	S1-6	CHANNEL
0	0	0	Invalid
0	0	1	CHANNEL 1: Do not set this (Reserved for standard RS)
0	1	0	CHANNEL 2: Do not set this (Reserved for noncontact clerk setting)
0	1	1	CHANNEL 3
1	0	0	CHANNEL 4
1	0	1	CHANNEL 5
1	1	0	CHANNEL 6:
1	1	1	CHANNEL 7: Do not set this (Reserved for internal printer)

② Terminating procedure

Press the Touch panel to terminate the check.

2) CH1 Check

① Check content

When the channel is not setting, an error is displayed (ERROR:CH1). When the channel is setting, the following check is performed.

- Control signal check

ERn	RSn	DRn	CIn	CDn	CSn
OFF	OFF	OFF	OFF	OFF	OFF
OFF	ON	OFF	OFF	ON	ON
ON	OFF	ON	ON	OFF	OFF
ON	ON	ON	ON	ON	ON

The read check of the above inputs and the interruption check of CS, CI, and CD are performed.

In the read check, ER and RS are changed over in the above sequence and the logic states of DR, CI, CD, and CS are checked.

If the logic differs from that in the table, an error display is made.

"ON" in the table means Active LOW, and "OFF" means Active HIGH.

In the interruption check, an interruption of CS, CI, or CD is allowed one by one. (The MASK is canceled.)

If an interruption is not made when each signal is active, or if an interruption is made when each signal is not active, an error display is made.

The above check is repeated in four cycles.

- Data transfer check

The loop back data (256 bytes) of 00H~0FFH are used for the data transfer check. The baud rate is set to 38400BPS.

- Timer check (RS232 on board timer)

Before performing the data transfer check, set the timer to RCVDT start and 5ms. Then perform the following procedure.

∗During execution of the data transfer check, TRQ- must not be generated.

∗After 5ms from completion of the data transfer check, TRQ- must be generated.

② Display

```
RS232 CH1 Check

   ER-DR          :   ERROR!!
```

All the contents of an error must be displayed.

ERROR No.	ERROR display	ERROR content
1	ER-DR:ERROR	ER-DR LOOP ERROR
2	ER-CI:ERROR	ER-CI LOOP ERROR
3	RS-CD:ERROR	RS-CD LOOP ERROR
4	RS-CS:ERROR	RS-CS LOOP ERROR
5	CI INT:ERROR	CI interruption is not made.
6	CD INT:ERROR	CD interruption is not made.
7	CS INT:ERROR	CS interruption is not made.
8	TXEMP:ERROR	TXEMP is not set.
9	TXEMP INT:ERROR	TXEMP interruption is not made.
10	TXRDY:ERROR	TXRDY is not set.
11	TXRDY INT:ERROR	TXRDY interruption is not made.
12	RCVRDY:ERROR	RCVRDY is not set. (Reception enabled. TR-Q is generated during data transfer check)
13	RCVRDY INT:ERROR	RCVRDY interruption is not made.
14	SD-RD:ERROR	SD-RD LOOP ERROR (DATA ERROR)
15	SD-RD:ERROR	SD-RD LOOP ERROR (DATA ERROR, FRAMING ERROR, etc.)
16	TIMER:ERROR	TIMER ERROR (TMRQ is not set after completion of data transfer check.)
17	TIMER INT:ERROR	TRQ-1 interruption is not made.

③ Terminating procedure

Press the Touch panel to terminate the check.

3) CH3 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as the CH1 Check.

4) CH4 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as the CH1 Check.

5) CH5 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as the CH1 Check.

6) CH6 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as the CH1 Check.

7) CH8 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as the CH1 Check. However, set the baud rate as 115200BPS.

3-7. Liquid Crystal Display Diagnostics

The UP-3301 LCD display is checked.

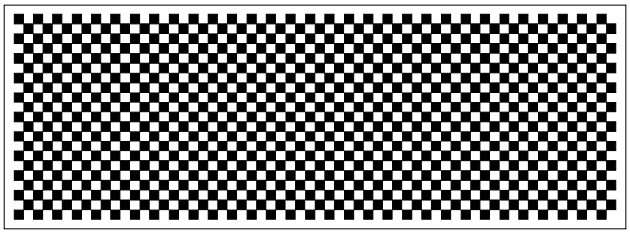
The test program displays the patterns in the following sequence. Every time the Touch panel is pressed, the next pattern is displayed. When the Touch panel is pressed at the final pattern the display to terminate the check.

1) Liquid Crystal Display Check

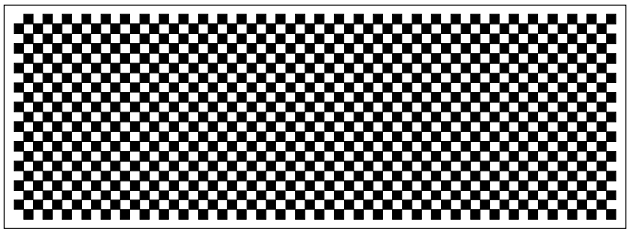
① Check content

The test patterns are displayed in the following sequence. When the Touch panel is pressed, the next pattern is displayed.

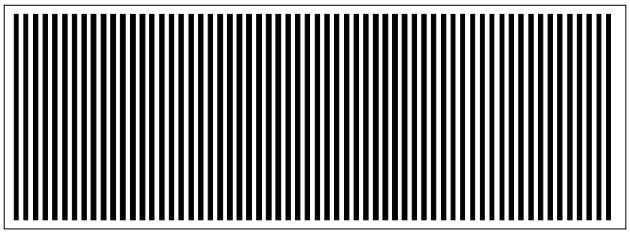
i. Black and white pattern at 1 dot pitch



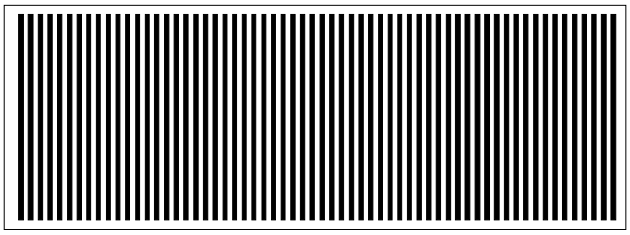
ii. Reversed pattern of the above (i)



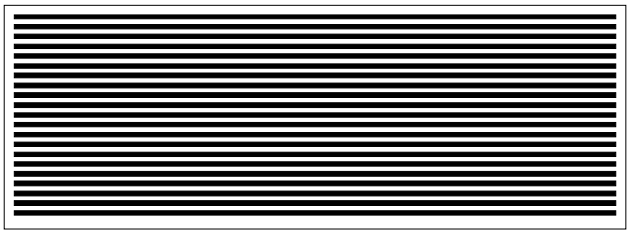
iii. Vertical stripe pattern at 1 dot pitch



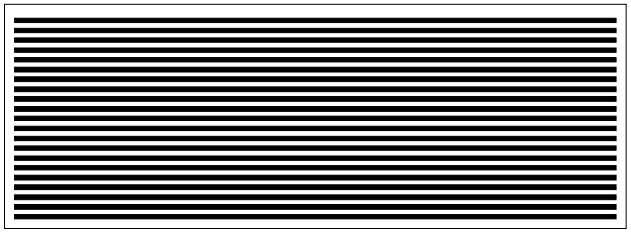
iv. Reversed pattern of the above (iii)



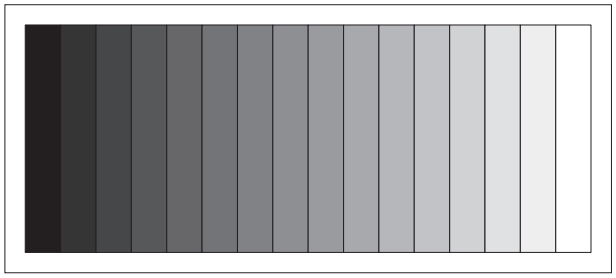
v. Horizontal stripe pattern at 1 dot pitch



vi. Reversed pattern of the above (v)

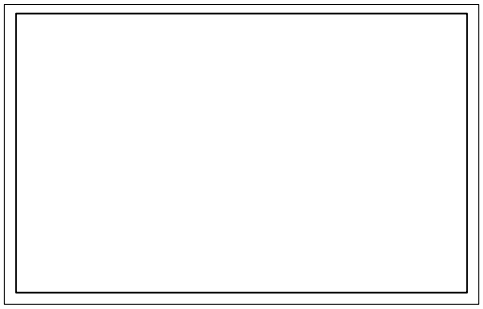


vii. Sixteen patterns of gradation ranging from black to white are displayed from left to right of the screen.



viii. 16-color bars are displayed.from left: black, blue, green, cyan, red, magenta, brown, white, gray, light blue, light green, light cyan, light red, light magenta, light yellow, and light white

ix. The outermost peripheral of the LCD's active area is displayed in one-dot line.



White raster test

x. "H" pattern. "H" is displayed in 80 digits and 25 lines. The 25th line only has 39 digits of "H."

HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
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HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH
HHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHHH

③ Terminating procedure

Press the Touch panel at the final pattern, terminate the check.

3-8. Rear Display Diagnostics

The rear display UP-I16DP or option display UP-P16DP is checked.

The test program displays the following patterns. When the Touch panel is pressed, the display returns to the diagnostics menu.

1) Rear Display Check

① Check content

The display test of the rear display is performed.

The test patterns are displayed in the following sequence. When the Touch panel is pressed, the next pattern is displayed.

i. The test pattern below is displayed.

ALPHA DISPLAY: 0 1 2 3 4 5 6 7 8 9 ; A a B b C

7-SEG DISPLAY: 0. 1. 2. 3. 4. 5. 6. 7. 8. 9. -.

ii. The test pattern with all the elements ON is displayed.

ALPHA DISPLAY: ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■ ■

7-SEG DISPLAY: 8. 8. 8. 8. 8. 8. 8. 8. 8. 8. 8.

② Display

Rear Display Check

③ Terminating procedure

Press the Touch panel to turn off all the elements of the rear display.

3-9. TCP/IP Stack Network Diagnostics

Performing the TCP/IP STACK test.

To perform this test, the following configuration is required.

- UP-3301
- 10BASE-T cable (only for data transmission test)
- HUB (only for LOOPBACK test and data transmission test when using satellites.)

The following menu is displayed. Touch the key of the operation you want to execute. After the individual program is completed, the screen returns to this menu. Press Cancel key to return to the Diag Main menu.

TCP/IP STACK Network Diagnostics

SELF Check	
LOOPBACK Check	
MAC ADDR&FIRM Ver. Read	
MAC ADDR&FIRM WRITE	
DATA Trans. (MA)	
DATA Trans. (SA)	
	Cancel

1) SELF Check

① Check content

The diagnostics is built in the FlashROM of the TCP/IP is executed in sequence and the result is displayed.

i. Executes the FLASH MEMORY TEST command and displays the result.

ii. Executes the SRAM TEST command and displays the result.

iii. Executes the DUALPORT-RAM TEST command and displays the result.

iv. Executes the INTERRUPT TEST command and displays the result.

The description of each error status is shown below.

b7: Reserved ("0" is always displayed.)

b6: Reserved ("0" is always displayed.)

b5: Reserved ("0" is always displayed.)

b4: Reserved ("0" is always displayed.)

b3: HR_RST : In case that /INTHR can not be reset, "1" is set.

b2: HR_ACK : In case that /INTHR is not received within 10ms, "1" is set.

b1: HW_RST : In case that /INTHR can not be reset, "1" is set.

b0: Reserved ("0" is always displayed.)

② Display

```
SELF Check
FLASH : PASS (or ERROR)
SRAM : PASS (or ERROR)
XXXXXXXX : XX : XX          ←address and data are displayed
                              when an error occurs.
DPRAM : PASS (or ERROR)
XXXXXXXX : XX : XX          ←address and data are displayed
                              when an error occurs.
INTERRUPT : PASS (or ERROR)
XXXXXXXX                    ←data is displayed when an error
                              occurs.
```

③ How to terminate

Press the Touch panel to terminate.

2) LOOPBACK Check

① Check content

Connect the RJ45 connector and the hub with a straight cable and execute the LOOPBACK TEST command to perform a 1 packet transmission.

② Display

```
LOOPBACK Check
LOOPBACK : PASS (or ERROR)
LOOPBACK ERROR              ←Displays when an error occurs.
LAN ERROR                   ←Displays when an error occurs.
```

③ How to terminate

Press the Touch panel to terminate.

3) MAC ADDRESS & FIRM Ver. read Check

① Check content

Reads the MAC Address and the firmware version and displays the content.

② Display

```
MAC ADDR&FIRM Ver.Read
MAC ADDRESS :
XX XX XX XX XX XX            ←Displays 6 BYTE information
FIRMWARE VERSION :
XXXXXXXX                     ←Displays 10 digits.
```

③ How to terminate

Press the Touch panel to terminate.

4) MAC ADDRESS & FIRM Write

① Operation content

Write MAC Address and the firmware.

(operation procedure)

- Install EPROM in ROM socket of TCP/IP and set IPL switch of TCP/IP to "program rewriting mode".
- Power on the UP-3301, then execute the MAC ADDR&FIRM WRITE diag.
- Enter three sets of three digits decimal from numeric key of touch panel, and touch the ENTER key.
- Write the MAC ADDRESS of total 6 byte, which is comprising SHARP maker code (08, 00, 1F) and the hexadecimal digits converted from three numbers entered with keyboard, into dual port RAM (800000H~)
- Turn the power off and remove the EPROM from the ROM socket of the TCP/IP, then set the IPL switch to "normal MODE".
- Power on the main unit.

Input: DUAL PORT RAM (80000H~)

08	00	1F	XX	YY	ZZ									

MAC ADDRESS (XX,YY,ZZ are in hexadecimal converted from decimal.)

Output: DUAL PORT RAM (800800H~)

- Rewriting

I	P	L		0	0	-	0	7					0	0

- When terminating (the same when a copy is skipped on the first verify.)

I	P	L		0	0	-	0	7					O	K

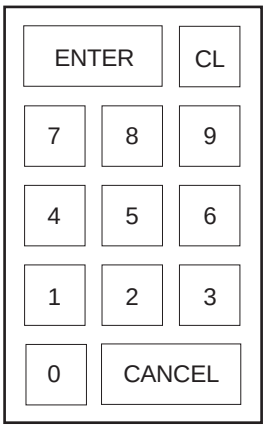
- When an error is terminated.

I	P	L		0	0	-	0	7					N	G

② Display

```
MAC ADDR&FIRM Write
MAC ADDRESS :
AAA BBB CCC                  ←Input with keyboard in decimal.
08 00 1F XX YY ZZ            ←Displays 6 BYTE in hexadecimal.
TCP/IP FIRM CHANGE :
IPL 00-07    XX (XX : 00~07 OK or NG)
```

To enter numbers, the numeric key panel is displayed in the lower part of the screen.



When the IPL switch is not in the writing MODE, the following message is displayed.

```
MAC ADDR&FIRM Write
CHANGE IPL SW!!
```

③ How to terminate

Press the Touch panel to terminate.

5) Data Transmission Check

Data transmission is checked in the system already established. The system is composed of one master machine and a max of 63 satellite machines.

Note when starting the test:

- When checking the set in which the LAN setting has been completed, disable the LAN setting before starting this check.
- When testing the system already established, disconnect the LAN cable of the sets not subject to test, or disable the LAN setting. Leaving LAN enabled may cause data to be destroyed.
- The transmission test setting must be performed after disabling the LAN setting of all the sets in the system. For the transmission check setting, first, set the satellite machines, then set the master machine.

UP-3301 DIAG uses private IP address. This DIAG assigns Private IP addresses to 64 terminal numbers to simplify the test as shown below. When performing data transmission check, be sure to physically disconnect other network where these IP addresses are set.

TERMINAL NO.1 = 192.168.0.1
TERMINAL NO.2 = 192.168.0.2
. . . . .
TERMINAL NO.63 = 192.168.0.63
TERMINAL NO.64 = 192.168.0.64

① How to set

i. Satellite machine setting

In the menu screen, select "Data Trans. (SA)". Following screen appears. Numeric key panel to enter numbers is displayed in the lower part of the screen.

```
Data Trans. (SA)
INPUT SA T-NO :  ←Enter one number out of 1 to 64.
```

Press the terminal No. (2 digits number between 1~64) of the machine to be checked and touch the Enter key.

The following screen appears.

```
Data Trans. (SA)
INPUT SA T-NO : XX      ←Displays the entered terminal numbers
                          of the satellite machine.
DATA SEQ NO. : 0000
```

ii. Master machine setting

In the menu screen, select "DATA Trans. (MA)". The following screen appears. Numeric key panel to enter numeric character is displayed in the lower part of the screen.

```
Data Trans. (MA)
INPUT MA T-NO :  ←Enter one number out of 1 to 64.
```

Press the terminal No.(2 digits number among 1~64) of the machine to be checked and Enter key.

The following screen appears. The numeric key panel to enter numeric characters is displayed in the lower part of the screen.

```
Data Trans. (MA)
INPUT MA T-NO : XX  ←Displays the entered terminal number of
                      the master machine.
INPUT SA T-NO :     ←Enter one number out of 1 to 64.
```

Press the terminal No. (2 digits number among 1~64) of the satellite machine to be connected to the test machine. The numeric key panel to enter numeric characters is displayed in the lower part of the screen.

```
Data Trans. (MA)
INPUT MA T-NO : XX          ←Displays the entered terminal
                              number of the master machine.
INPUT SA T-NO : XX (or XXXX) ←Displays the entered terminal
                              numbers of the satellite machine.
```

When checking with two or more satellite machines connected, repeat the entry for the terminal No. (2 digits, 1~64) and touch ENTER key. To execute the checking, touch the ENTER key without entering the terminal No. You can also enter the terminal No. with range designating function without entering all terminal No. After entering the first terminal No. and last terminal No. of the satellite machine, touch ENTER key. For example, when you want to enter the terminal No. 5~63 of the satellite machine, touch "0515" and ENTER key.

The following screen appears.

```
Data Trans. (MA)
INPUT MA T-NO : XX  ←Displays the entered terminal number of
                      the master machine.
INPUT SA T-NO : XX  ←Displays the entered terminal number of
                      the satellite machine.
 XX XX XX XX XX XX (or XXXX)   When multiple terminal number
DATA SEQ.NO. : 0000            of the satellite machine are
                               entered, all of them will be dis-
                               played.
```

Do not assign the same terminal No. to different machines (master/satellite).

When you designate terminal No. with range designating function, the terminal No. used in the master machine is excluded from the designated terminal number of the satellite machine.

After completing the above setting, data transmission test starts.

② Check content

i. Data composed of 2 byte sequence No. and 254 byte AAH data in the following format are transmitted from the master machine to the satellite machine. The master machine displays the sequence No.

Test data format (1 packet : 256 byte)

1	2	3	4	5	···	···	···	254	255	256	Byte
XX	XX	AA	AA	AA	···	···	···	AA	AA	AA	

XXXX : Sequence No. (2byte: 4digits of binary decimal numbers)
AA : Transmission data (AAH) x 254 bytes

ii. The satellite machine sends back the received data to the master machine. The satellite machine displays the received sequence No.

iii. After receiving the data, the master machine checks the sequence No. and 254 byte AAH data. In case of an error, the error code is displayed and the test is completed. If multiple satellite machines are connected, the step i and ii above operation are repeated. If data transmission with all the satellite machines are normally completed, the master machine increments the sequence No.

Repeat step i and iii.

③ Error display

Data Trans. (MA)
INPUT MA T-NO : XX
INPUT SA T-NO : XX
XX XX XX XX XX XX
XX XX XX XX XX XX (or XXXX)
DATA SEQ.NO. : 0000
TCP/IP ERROR : XX ←Displays ERROR CODE.

Description of the error codes are shown below. (comply with TCP/IP HDNLER)

01	Improper command (except when transmission)
02	No data received.
03	Received data present. Received data remained.
04	Remote machine not ready (when sending) "NTDY" is sent back because the remote machine is not ready for reception.
05	Received buffer full (when sending) The controller's receive buffer of the remote machine is full.
06	Re-send error (when sending) Excess retrying (5 times) for no response
07	Collision error (when sending) In a collision circumstance, excess in retry times (16 times) for re-collision after a random (0~255ms) interval.
08	Line busy time out. Transmission can not be made due to the communications between multi-station, and it causes time out in data send wait time.
09	Excess of allowed receive size (when receiving) Received buffer size is insufficient.
0A	Hardware error Improper interface (LAN controller etc.)

④ How to terminate

Touch PANEL key to terminate the check.

3-10. Magnetic Card Reader Diagnostics

Read check of the optional UP-E12MR2 is performed.

The test program reads the magnetic card of ISO 7811/1-5 standard and displays the data. When the Touch panel is pressed, the display returns to the diagnostics menu.

1) Magnetic Card Reader Check

① Check content

The test program reads tracks 1 and 2 of the magnetic card of ISO 7811/1-5, and displays the data in ASCII code.

② Display

MCR (Magnetic Card Reader) Check

TRACK1:
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
xxxxxxxxxx
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
TRACK2:
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

XXXXX shows the data read by the MCR. Incase of an error, the error code is displayed as shown below.

Magnetic Card Reader Check

TRACK1:BUFFEREMPTY	- Displayed when TRACK1 empty code is sent back.
TRACK1:MCRERROR	- Displayed when TRACK1 error code is sent back.
TRACK2:BUFFEREMPTY	- Displayed when TRACK2 empty code is sent back.
TRACK2:MCRERROR	- Displayed when TRACK2 error code is sent back.

③ Terminating procedure

Press the Touch panel to terminate the check.

3-11. Drawer Diagnostics

This diagnostics is used to check the drawer open and sensors.

The following menu is displayed. Press the position of the operation you want to perform to execute individual Diag programs.

Pressing the CANCEL key returns the screen to the Diag MAIN menu.

Drawer Diagnostics

Drawer 1 Check	
Drawer 2 Check	
	Cancel

1) Drawer 1 Check

① Check content

The solenoid of drawer 1 is turned on, and the drawer open sensor value is sensed at every 100ms, and the state is displayed.

② Display

```
Drawer1 Check

  Drawer Open Sensor          : OPEN (or CLOSE)
```

③ Terminating procedure

Press the Touch panel to terminate the check.

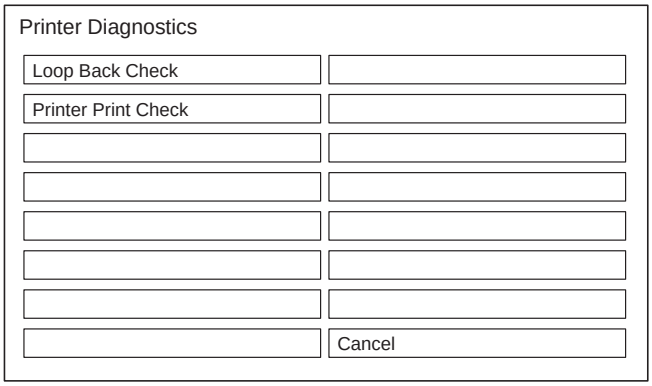
2) Drawer 2 Check

① Check content

The solenoid of drawer 2 is turned on, and the drawer open sensor value is sensed at every 100ms, and the state is displayed.
The display and the terminating procedure are the same as Drawer 1 Check.

3-12. Printer Diagnostics

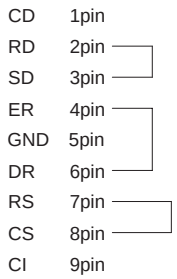
I/F loopback and printing tests of the built-in printer are performed.
The following menu appears. Press the name of the test you want to perform to execute its Diag program. When the Diag program is terminated, the screen returns to the Printer Diagnostics menu. Pressing the CANCEL key returns to screen to the Diag Menu.



1) Loop Back Check

① Check content

A LOOPBACK test on the built-in printer (UP-T80BP) interface (logic channel 7 of RS232) is performed and the result is displayed. The test itself is the same as that for the RS232. The difference in test specifications is as follows: The loopback signals are for ER-DR, RS-CS, TXD-RXD only and the following LOOPBACK-Connectors are required.



Wiring diagram of loopback connectors
(UKOG-2356BHZZ)

② Indication

The indication is the same as that for RS232 DIAGNOSTICS.

③ End

Press the PANEL to end the program.

2) Printer Print Check

① Check

Send the signal to generate a receipt (by DIAG COMMAND) to the UP-T80BP.

3-13. EFT Diagnostics

Check of the EFT (ER-02EF) is performed.
Select the EFT Diag, and turn of the power supply after that.

```
EFT Diagnostics
```

1) EFT Check

Set all the bits of DIPSW1 to “off”, then turn off the power supply of main unit. The EFT check is performed automatically.

① Check content

i. Executes the LOOP BACK TEST to EFT connector about ER-DR, ER-CT and RS-CS signals.

ii. Executes the DIPSW1 check by turning on the 1-8 bit of DIPSW1 in order.

iii. When normal, SUM CHECK of EFT ROM is performed automatically, and WRITE/READ check is performed to RAM.

② Display (Normal)

```
DIAGO (SELF TEST) : OK
VHI27040R**1*     : OK
256K SRAM         : OK
```

③ Display (Error)

```
In Loop Back Error
  ER-DR LOOP ERROR
  ER-CI LOOP ERROR
  ER-CS LOOP ERROR
In Self Test Error
  DIP SW ERROR
In Self Test Error
  VHI27040R**1*   : ERROR
  256K SRAM       : ERROR
```

④ End

Pless the PANEL to end the program.

3-14. Contactless CLERK Diagnostics

The contactless CLERK key code is read. The self check of the contactless CLERK key is also performed.

When the contactless CLERK Diag. is performed, the following menu is displayed. Put the cursor on the item to be executed, and press the ENTER key to perform the individual diagnostic program. When the CANCEL key is pressed, the display returns to the diagnostic menu.

Contactless CLERK Diagnostics

SELF Check	
KEY READ Check	
FIRM Write	
	Cancel

1) Self Check

① Check content

The self check and the firmware version check are performed for the contactless CLERK connected to RS232 CH2.

②Display

```
Contactless CLERK SELF CHECK
   SELF CHECK : PASS (or ERROR)
   FIRMWARE VERSION : xx   ←1 byte display
```

③ Termination

After completion of the check, press the CANCEL key to terminate the check.

2) Key Read Test

① Check content

The read command of the key is sent and the contactless CLERK key code is displayed in hexadecimal number. The machine stands by under the reception state. If the key status is changed, the received key code is displayed.

②Display

```
KEY READ TEST
   KEY CODE = 0000000060D2E07B
```

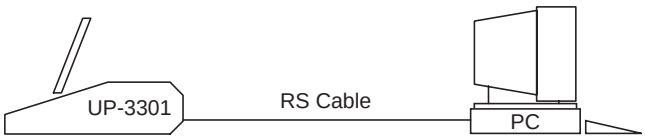
③ Termination

After completion of the check, press the CNACEL key to terminate the check.

3) FIRM Write

① Operations

This diagnostic is used to write the firmware of the contactless CLERK. By use of the firmware writing tool on the PC side, the contactless CLERK firmware is written. The composition is as follows:



Contactless CLERL key FIRM wite

The machine and the PC are connected with an RS cable.

(Operating procedure)

- Connect CH1 of the UP-3301 and the PC with the RS cable, and turn on the power.
- Execute the firmware writing program on the PC side.
- Select “Contacless CLERK Diag.” on the diagnostic menu, and execute “FIRM Write.”
- The password entry menu is displayed. Enter the password of “11111111” (8 digits).
- Firmware data are received from the PC side and writing is performed.
- When writing is completed normally, the self check is performed and the firmware version is displayed and the check is terminated normally.
- Press the CANCEL key to terminate the diagnostic, and the display returns to the initial menu.

② Display

```
Contactless CLERK FIRM Wire


PASSWORD = XXXXXXXX          ←Enter the pass word of
                               "11111111! (8 digits).
FIRM CHANG:
IPL 00-12  XX (XX:00~12 OK or NG)
FIRMWARE VERSION: XX         ←One byte of the version is
                               displayed.
```

- Rewriting

I	P	L		0	0	-	1	2					0	0

- When completing

I	P	L		0	0	-	1	2					O	K

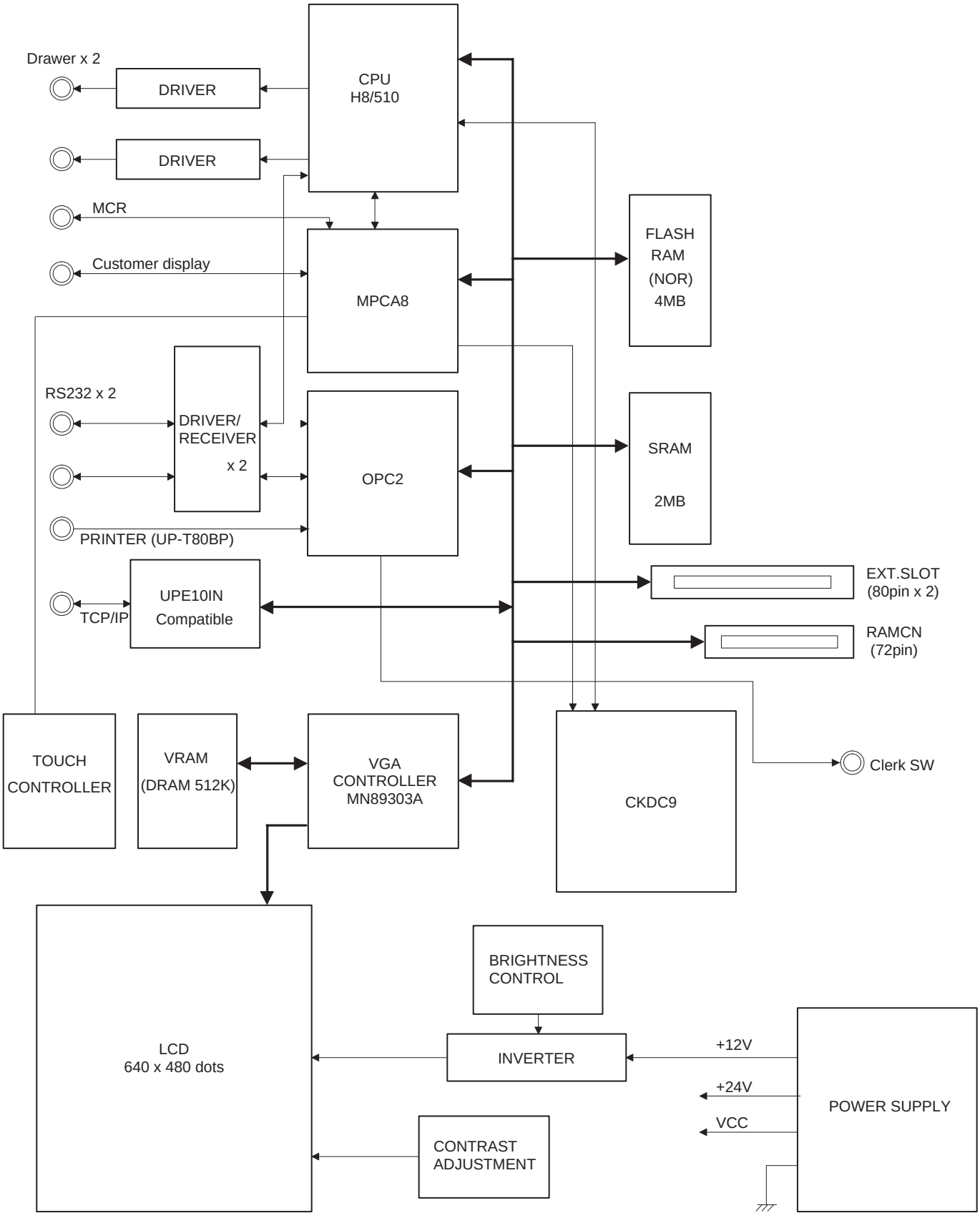
- When error completing

I	P	L		0	0	-	1	2					N	G

③ Press the CANCEL key to terminate the check.

CHAPTER 7. CIRCUIT DESCRIPTION

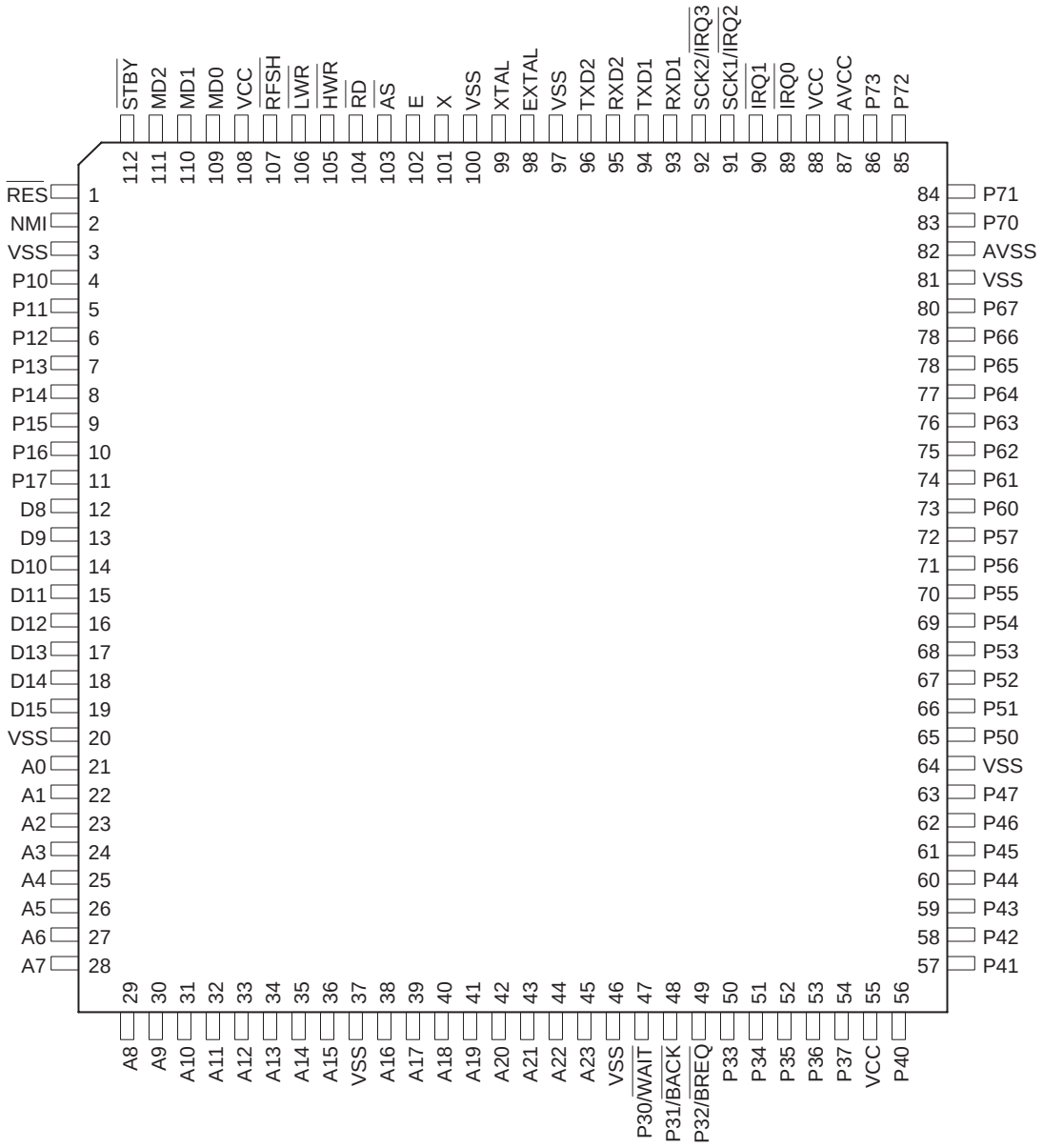
1. Hardware block diagram



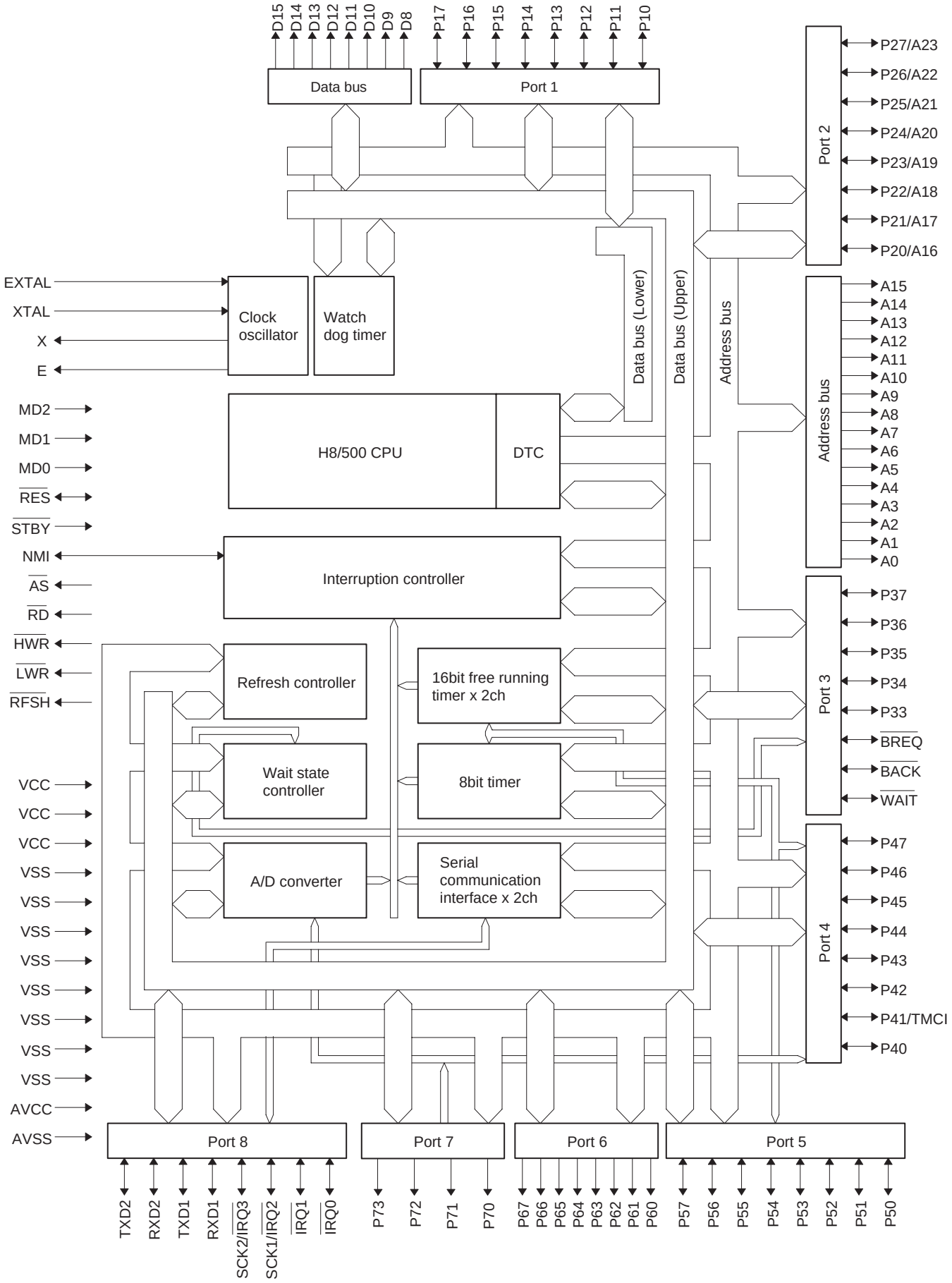
2. Description of main LSI's

2-1. CPU (HD6415108FX)

1) Pin description



2) Block diagram

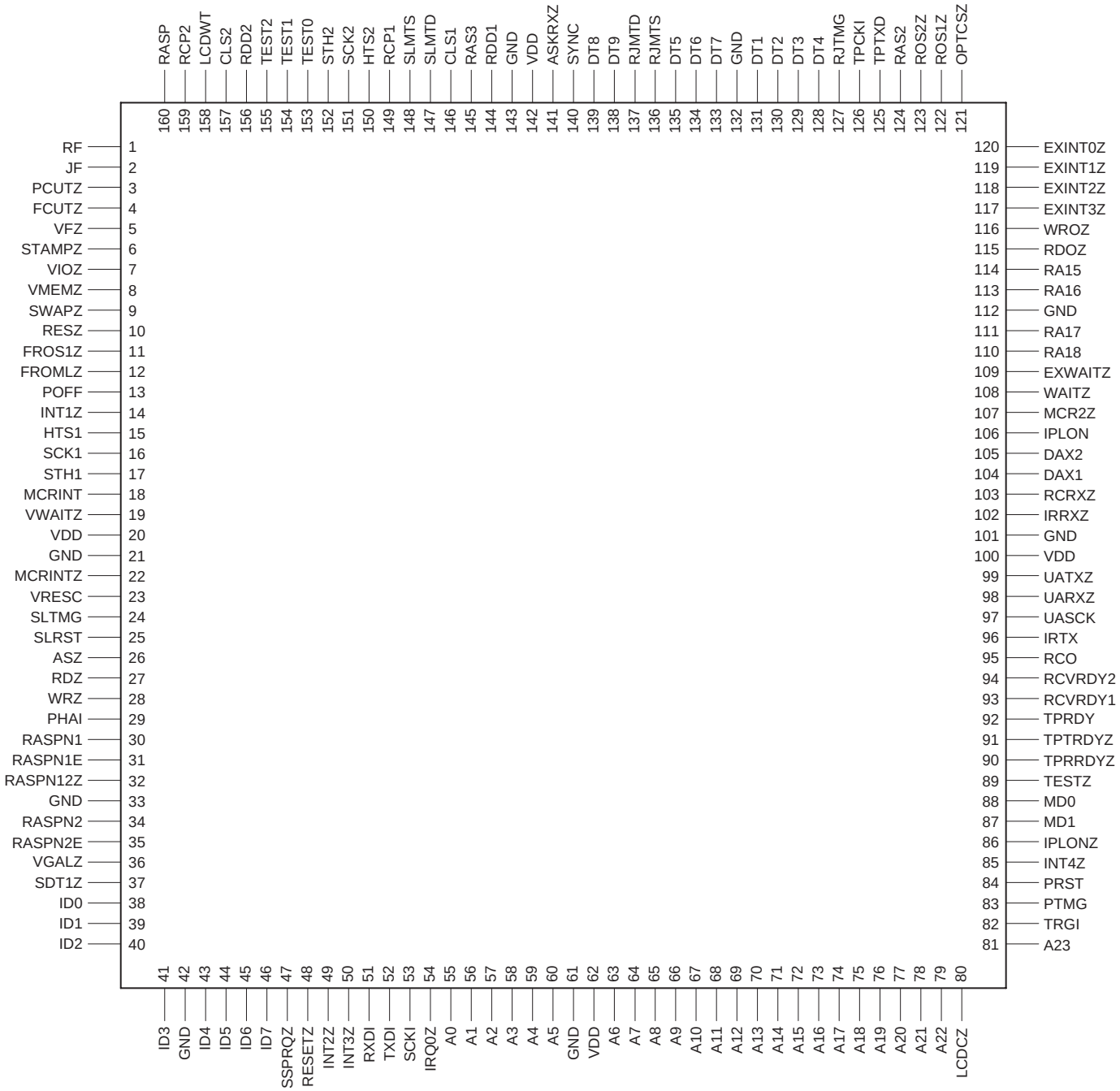


3) Pin description

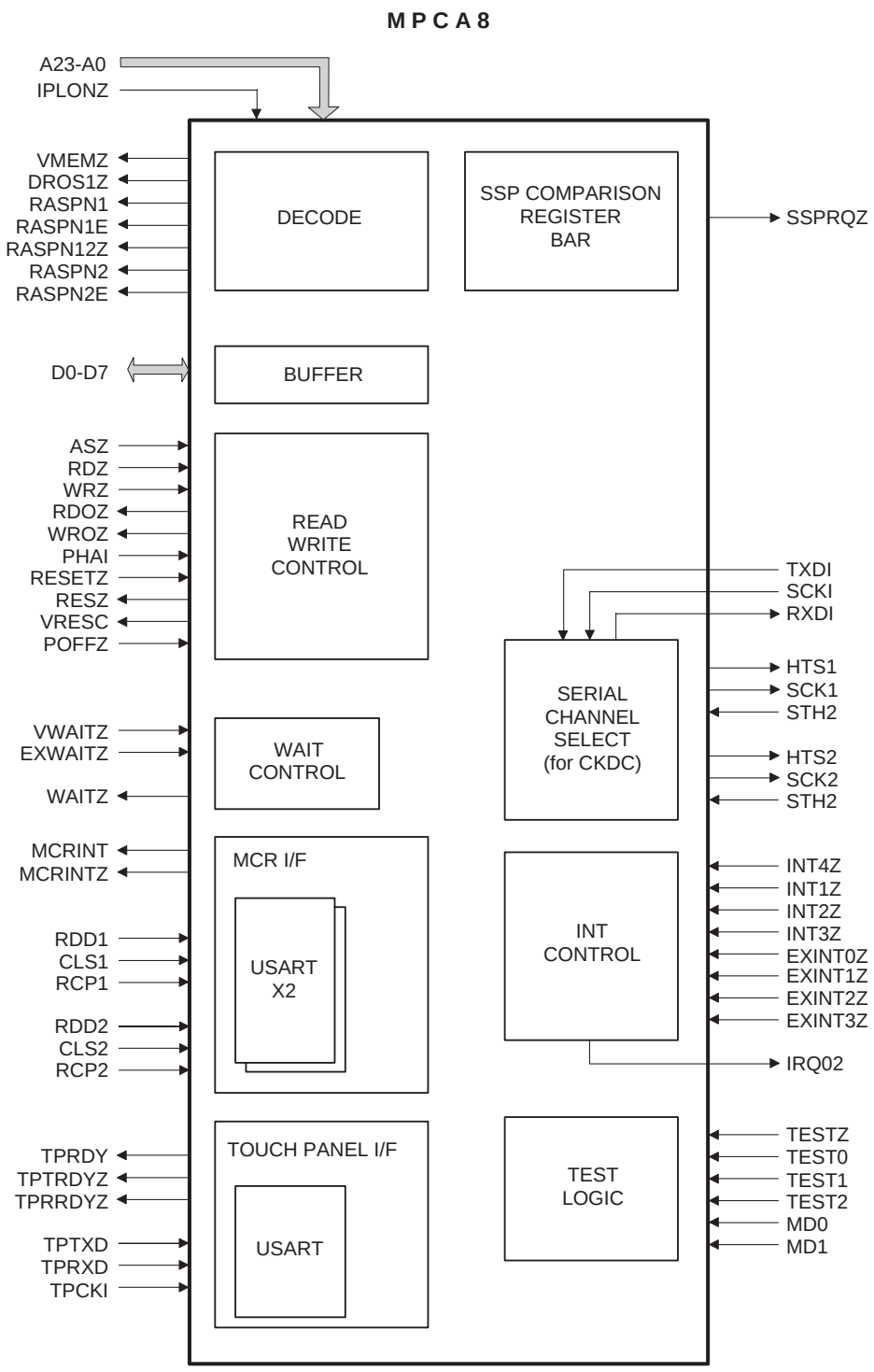
Pin No.	Symbol	Signal name	In/ Out	Function
1	/RES	/RESET	In	Reset signal
2	NMI	NMI	In	Non-maskable interrupt input for SSP interrupt input.
3	VSS	GND	In	GND
4	D0	D0	I/O	Data bus
5	D1	D1	I/O	Data bus
6	D2	D2	I/O	Data bus
7	D3	D3	I/O	Data bus
8	D4	D4	I/O	Data bus
9	D5	D5	I/O	Data bus
10	D6	D6	I/O	Data bus
11	D7	D7	I/O	Data bus
12	D8	D8	I/O	Data bus
13	D9	D9	I/O	Data bus
14	D10	D10	I/O	Data bus
15	D11	D11	I/O	Data bus
16	D12	D12	I/O	Data bus
17	D13	D13	I/O	Data bus
18	D14	D14	I/O	Data bus
19	D15	D15	I/O	Data bus
20	VSS	GND	In	GND
21	A0	A0	Out	Address bus
22	A1	A1	Out	Address bus
23	A2	A2	Out	Address bus
24	A3	A3	Out	Address bus
25	A4	A4	Out	Address bus
26	A5	A5	Out	Address bus
27	A6	A6	Out	Address bus
28	A7	A7	Out	Address bus
29	A8	A8	Out	Address bus
30	A9	A9	Out	Address bus
31	A10	A10	Out	Address bus
32	A11	A11	Out	Address bus
33	A12	A12	Out	Address bus
34	A13	A13	Out	Address bus
35	A14	A14	Out	Address bus
36	A15	A15	Out	Address bus
37	VSS	GND	In	GND
38	A16	A16	Out	Address bus
39	A17	A17	Out	Address bus
40	A18	A18	Out	Address bus
41	A19	A19	Out	Address bus
42	A20	A20	Out	Address bus
43	A21	A21	Out	Address bus
44	A22	A22	Out	Address bus
45	A23	A23	Out	Address bus
46	VSS	GND	In	GND
47	P30	/WAIT	In	Wait signal
48	P31	/BACK	Out	Bus control request acknowledge signal
49	P32	/BREQ	In	Bus control request signal
50	P33	DOPS	In	Drawer open signal
51	P34	/DR0	Out	Option drawer open signal
52	P35	/DR1	Out	Option drawer open signal
53	P36	NC	NC	NC
54	P37	NC	NC	NC
55	VCC	VCC	In	+5V
56	P40	VCC	In	+5V
57	P41	GND	In	GND
58	P42	GND	In	GND
59	P43	GND	In	GND
60	P44	MCRINT	In	MCR interrupt signal
61	P45	GND	In	GND
62	P46	/SHEN	In	CKDC interface shift enable signal
63	P47	GND	In	GND
64	VSS	GND	In	GND
65	P50	/ER	Out	DTR signal for RS-232 CH8
66	P51	/DR	In	DSR signal for RS-232 CH8
67	P52	/CS	In	CTS signal for RS-232 CH8
68	P53	/CD	In	DCD signal for RS-232 CH8
69	P54	/RR	Out	RR signal for RS-232 CH8
70	P55	/RS	Out	RTS signal for RS-232 CH8
71	P56	/CI	In	RI signal for RS-232 CH8
72	P57	GND	Out	GND
73	P60	/IPLON0	In	From IPL SW of ER-A7RS2
74	P61	/IPLON1	In	From IPL SW of UP-3301
75	P62	/SRESET	In	TCP/IP RESET signal
76	P63	NORDY	In	Flash Memory ready (“H” active)
77	P64	FVPON	Out	Flash Memory write protect (“L” active)
78	P65	BANK	Out	For IPL ROM
79	P66	/CLRES	Out	Clerk key reset output signal
80	P67	/STOP	Out	System reset output signal
81	VSS	GND	In	GND
82	AVSS	GND	In	GND
83	P70	GND	In	GND
84	P71	GND	In	GND
85	P72	GND	In	GND
86	P73	GND	In	GND
87	AVCC	VCC	In	+5V
88	VCC	VCC	In	+5V
89	/IRQ0	/IRQ0	In	Interrupt signal 0
90	/IRQ1	/IRQ1	In	Interrupt signal 1
91	/IRQ2	UASCK	In	Synchronizing shift clock signal for IR
92	/IRQ3	SCKI	Out	CKDC interface synchronizing shift clock
93	RXD1	/UARX	In	RXD signal for RS-232 CH8
94	TXD1	/UATX	Out	TXD signal for RS-232 CH8
95	RXD2	RXDI	In	CKDC interface shift input data
96	TXD2	TXDI	Out	CKDC interface shift output data
97	VSS	GND	In	GND
98	EXTAL	EXTAL	In	Crystal oscillator connection 19.6MHz
99	XTAL	XTAL	In	Crystal oscillator connection 19.6MHz
100	VSS	GND	In	GND
101	X	#	Out	System clock
102	E	NC	NC	NC
103	/AS	/AS	Out	Address strobe
104	RD	/RD	Out	Read signal
105	/HWR	/HWR	Out	Write signal (HIGH)
106	/LWR	/LWR	Out	Write signal (LOW)
107	/RFSH	/RFSH	Out	Refresh cycle signal
108	VCC	VCC	In	+5V
109	MD0	IPLON0	In	From IPL SW of ER-A7RS2
110	MD1	IPLON0	In	From IPL SW of ER-A7RS2
111	MD2	/IPLON0	In	From IPL SW of ER-A7RS2
112	/STBY	VCC	In	+5V

2-2. G.A.(MPCA8)

1) Pin configuration



2) Block diagram



3) Pin description

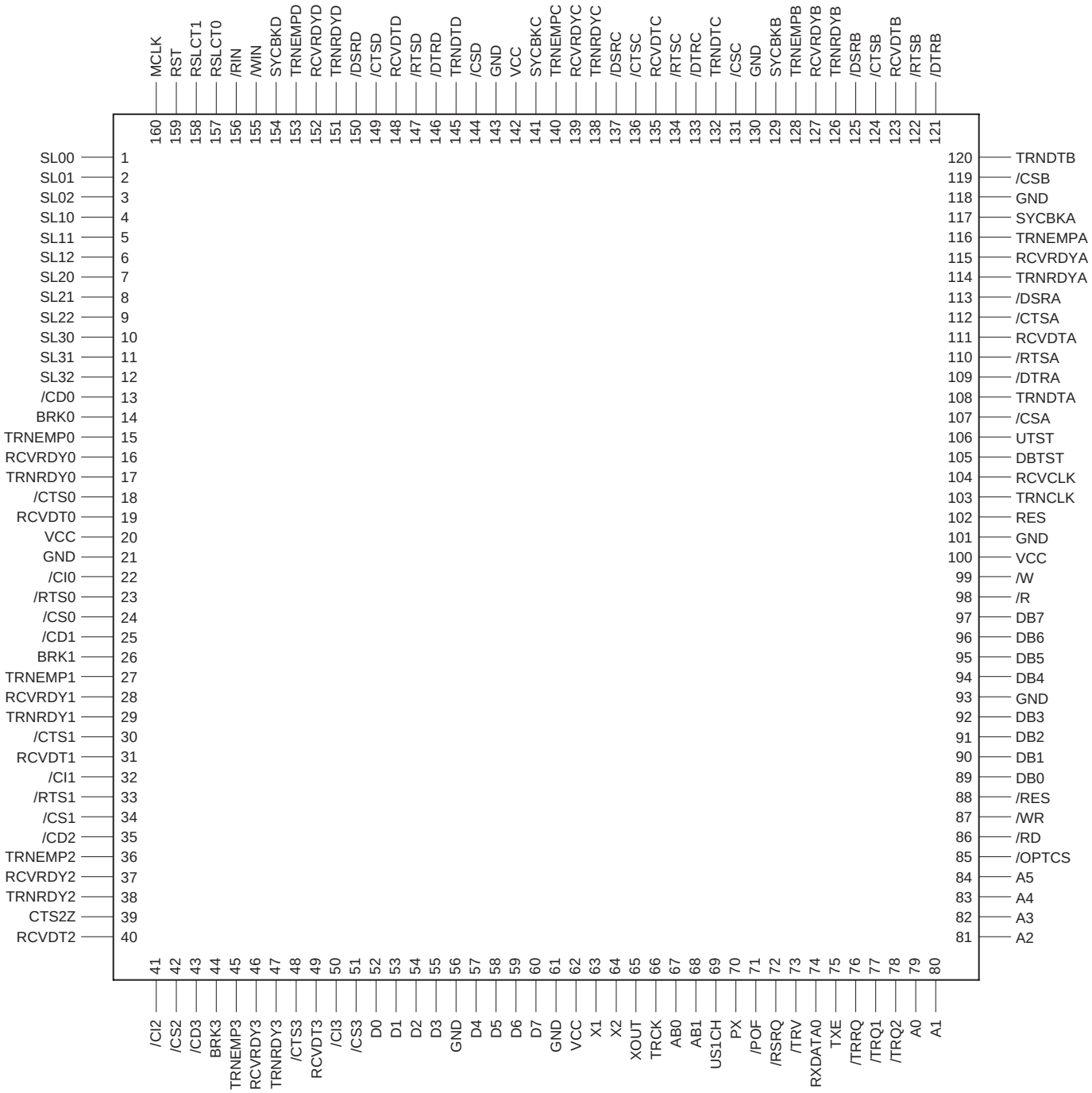
Pin No.	Name	I/O	Description
1	RF	ON	NU
2	JF	ON	NU
3	PCUTZ	ON	NU
4	FCUTZ	ON	NU
5	VFZ	ON	NU
6	STAMPZ	ON	NU
7	VIOZ	O	NU
8	VMEMZ	O	VRAM DECODER
9	SWAPZ	O	NU
10	RESZ	O6M	RESET
11	FROS1Z	O	FLASH ROM DECODER
12	FROMLZ	O	NU
13	POFF	IC	POWER OFF SIGNAL INPUT
14	INT1Z	ICU	INTERRUPT SIGNAL INPUT
15	HTS1	O	SERIAL OUT (CKDC INTERFACE)
16	SCK1	O	SERIAL CLOCK (CKDC INTERFACE)
17	STH1	IS	SERIAL IN (CKDC INTERFACE)
18	MCRINT	O	MCR INTERRUPT OUT
19	VWAITZ	IU	VGA WAIT INPUT
20	VDD	–	
21	GND	–	
22	MCRINTZ	O	MCR INTERRUPT OUT
23	VRESC	ON	TURNS ACTIVE WHEN RESET&POWER DOWN IS MET
24	SLTMG	ICS	GND
25	SLRST	ICS	GND
26	ASZ	I	ADDRESS STROBE
27	RDZ	I	READ STROBE
28	WRZ	I	WRITE STROBE
29	PHAI	IS	SYSTEM CLOCK (9.83MHz)
30	RASPN1	O	PSRAM DECODE1
31	RASPN1E	O	PSRAM DECODE1 (EVEN)
32	RASPN12Z	O	PSRAM DECODE1 OR 2
33	GND	–	
34	RASPAN2	O	PSRAM DECODE2
35	RASPN2E	O	PSRAM DECODE2 (EVEN)
36	VGALZ	O	NU
37	SDT1Z	O	NU
38	ID0	IO	DATA BUS
39	ID1	IO	DATA BUS
40	ID2	IO	DATA BUS
41	ID3	IO	DATA BUS
42	GND	–	
43	ID4	IO	DATA BUS
44	ID5	IO	DATA BUS
45	ID6	IO	DATA BUS
46	ID7	IO	DATA BUS
47	SSPRQZ	O	SSP REQUEST FOR CPU
48	RESETZ	ICS	MPCA RESET
49	INT2Z	ICU	INTERRUPT INPUT (/TPRRDY)
50	INT3Z	ICU	INTERRUPT INPUT (/TPTRDY)
51	RXDI	O	SERIAL OUT FOR CPU
52	TXDI	IS	SERIAL IN FROM CPU
53	SCKI	IU	SERIAL CLOCK FROM CPU
54	IRQ0Z	O	INTERRUPT SIGNAL FOR CPU
55	A0	I	ADDRESS BUS
56	A1	I	ADDRESS BUS
57	A2	I	ADDRESS BUS
58	A3	I	ADDRESS BUS
59	A4	I	ADDRESS BUS
60	A5	I	ADDRESS BUS
61	GND	–	
62	VDD	–	
63	A6	I	ADDRESS BUS
64	A7	I	ADDRESS BUS
65	A8	I	ADDRESS BUS
66	A9	I	ADDRESS BUS
67	A10	I	ADDRESS BUS
68	A11	I	ADDRESS BUS
69	A12	I	ADDRESS BUS
70	A13	I	ADDRESS BUS
71	A14	I	ADDRESS BUS
72	A15	I	ADDRESS BUS
73	A16	I	ADDRESS BUS
74	A17	I	ADDRESS BUS
75	A18	I	ADDRESS BUS
76	A19	I	ADDRESS BUS
77	A20	I	ADDRESS BUS
78	A21	I	ADDRESS BUS
79	A22	I	ADDRESS BUS
80	LCDCZ	O	NU
81	A23	I	ADDRESS BUS
82	TRGI	IS	NU
83	PTMG	O	NU
84	PRST	O	NU
85	INT4Z	ICU	NU
86	IPLONZ	IU	IPL SIGNAL FROM OPTION CONNECTER
87	MD1	ICU	TEST PIN
88	MD0	ICU	TEST PIN
89	TESTZ	ICU	TEST PIN
90	TPRRDYZ	O	TOUCH PANEL INTERRUPT (CONNECTED TO INT2Z)
91	TPTRDYZ	O	TOUCH PANEL INTERRUPT (CONNECTED TO INT3Z)
92	TPRDY	O	NU
93	RCVRDY1	IU	NU
94	RCVRDY2	IU	NU
95	RCO	O	NU
96	IRTX	O	OUT
97	UASCK	O	CLOCK
98	UARXZ	O	DATA FOR CPU
99	UATXZ	IU	DATA FROM CPU
100	VDD	–	
101	GND	–	

Pin No.	Name	I/O	Description
102	IRRXZ	ICS	NU
103	RCRXZ	ICS	NU
104	DAX1	OSCI	NU
105	DAX2	OSCO	NU
106	IPLON	O	IPL ON SIGNAL
107	MCR2Z	O	NU
108	WAITZ	O	WAIT FOR CPU
109	EXWAITZ	IU	EXTERNAL WAIT INPUT SIGNAL
110	RA18	O	NU
111	RA17	O	NU
112	GND	–	
113	RA16	O	NU
114	RA15	O	NU
115	RDOZ	O8M	EXPANSION RD
116	WROZ	O8M	EXPANSION WR
117	EXINT3Z	ICS	EXPANSION INTERRUPT SIGNAL
118	EXINT2Z	ICS	EXPANSION INTERRUPT SIGNAL
119	EXINT1Z	ICS	EXPANSION INTERRUPT SIGNAL
120	EXINT0Z	ICS	EXPANSION INTERRUPT SIGNAL
121	OPTCSZ	O	BASE DECODE SIGNAL FOR EXPANSION SLOT
122	ROS1Z	O	NU
123	ROS2Z	O	NU
124	RAS2	O	NU
125	TPTXD	O	SERIAL OUT FOR TOUCH PANEL
126	TPRXD	ICS	SERIAL IN FROM TOUCH PANEL
127	TPCKI	ICS	SERIAL CLOCK 9.83MHz/64 (TOUCH PANEL INTERFACE)
128	DT4	ON	NU
129	DT3	ON	NU
130	DT2	ON	NU
131	DT1	ON	NU
132	GND	–	
133	DT7	ON	NU
134	DT6	ON	NU
135	DT5	ON	NU
136	RJMTS	ON	NU
137	RJMTD	ON	NU
138	DT9	ON	NU
139	DT8	ON	NU
140	SYNC	IU	NU
141	ASKRXZ	ICS	NU
142	VDD	–	
143	GND	–	
144	RDD1	ICS	SERIAL IN FROM MCR TRACK1
145	RAS3	O	NU
146	CLS1	ICS	CARD SENSE ON MCR TRACK1
147	SLMTD	ON	NU
148	SLMTS	ON	NU
149	RCP1	ICS	CLOCK PULSE FROM MCR TRACK1
150	HTS2	O	SERIAL OUT (OPTION CKDC INTERFACE) NU
151	SCK2	O	SERIAL CLOCK (OPTION CKDC INTERFACE) NU
152	STH2	IS	SERIAL IN (OPTION CKDC INTERFACE) NU
153	TEST0	I	TEST PIN
154	TEST1	I	TEST PIN
155	TEST2	I	TEST PIN
156	RDD2	ICS	SERIAL IN FROM MCR TRACK1
157	CLS2	ICS	CARD SENSE ON MCR TRACK1
158	LCDWT	IU	NU
159	RCP2	ICS	CLOCK PULSE FROM MCR TRACK1
160	RASP	O	NU

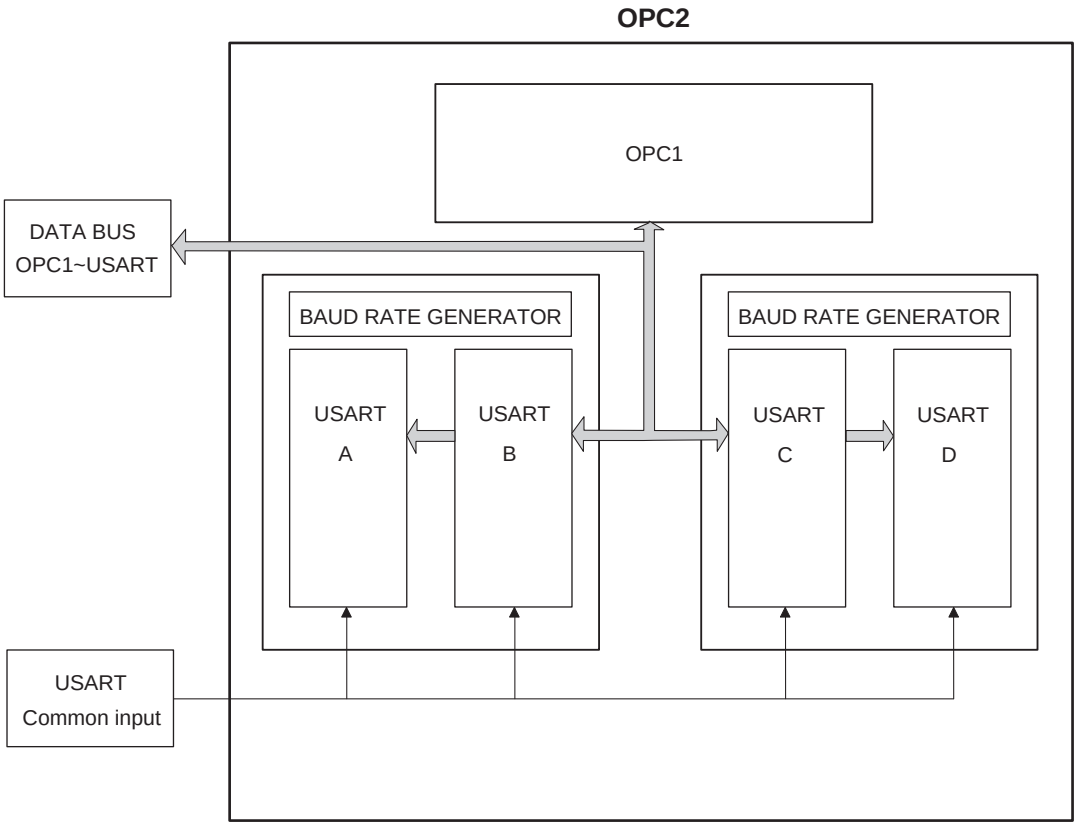
I	TTL input
IS	TTL Schmidt input
IU	TTL pull up input
IC	CMOS input
ICS	CMOS Schmidt input
ICU	CMOS pull up input
IO	TTL I/O
O	Output 4mA
O8M	Output 8mA
ON	Nch open drain output
OSIC	Oscillation circuit input
OSCI	Oscillation circuit output

2-3. OPC2

1) Pin configuration



2) Block diagram



3) Pin descriptions

Pin NO.	Name	UP-3301	I/O	Description
1	SL00	VCC	ISU	RS-232/UNIT0 channel select
2	SL01	GND	ISU	
3	SL02	GND	ISU	
4	SL10	GND	ISU	RS-232/UNIT1 channel select
5	SL11	VCC	ISU	
6	SL12	GND	ISU	
7	SL20	VCC	ISU	RS-232/UNIT2 channel select
8	SL21	VCC	ISU	
9	SL22	VCC	ISU	
10	SL30	GND	ISU	RS-232/UNIT3 channel select
11	SL31	GND	ISU	
12	SL32	GND	ISU	
13	/CD0	/DCD1	IS	RS-232 control signal /CD input
14	BRK0	BRK1	IS	RS-232 break signal
15	TRNEMP0	TRENMP1	IS	RS-232 transmission buffer empty signal
16	RCVRDY0	RCVRDY1	IS	RS-232 data reception enable signal
17	TRNRDY0	TRNRDY1	IS	RS-232 transmission enable signal
18	/CTS0	/CTS1	IS	RS-232 clear to send signal
19	RCVDT0	RCVDT1	IS	RS-232 reception data signal
20	VCC	VCC		+5V
21	GND	GND		GND

Pin NO.	Name	UP-3301	I/O	Description
22	/CI0	/CI1	IS	RS-232 control signal /CI input
23	/RTS0	/RTS1	O	RS-232 request to send signal
24	/CS0	/CS1	O	RS-232 chip select signal
25	/CD1	/DCD2	IS	RS-232 control signal /CD input
26	BRK1	BRK2	IS	RS-232 break signal
27	TRNEMP1	TRENMP2	IS	RS-232 transmission buffer empty signal
28	RCVRDY1	RCVRDY2	IS	RS-232 data reception enable signal
29	TRNRDY1	TRNRDY2	IS	RS-232 transmission enable signal
30	/CTS1	/CTS2	IS	RS-232 clear to send signal
31	RCVDT1	RCVDT2	IS	RS-232 reception data signal
32	/CI1	/CI2	IS	RS-232 control signal /CI input
33	/RTS1	/RTS2	O	RS-232 request to send signal
34	/CS1	/CS2	O	RS-232 chip select signal
35	/CD2	VCC	IS	+5V
36	TRNEMP2	TRENMP3	IS	RS-232 transmission buffer empty signal
37	RCVRDY2	RCVRDY3	IS	RS-232 data reception enable signal
38	TRNRDY2	TRNRDY3	IS	RS-232 transmission enable signal

Pin NO.	Name	UP-3301	I/O	Description
39	CTS2Z	/CTS3	IS	RS-232 clear to send signal
40	RCVDT2	RCVDT3	IS	RS-232 reception to send signal
41	/CI2	VCC	IS	+5V
42	/CS2	/CS3	O	RS-232 chip select signal
43	/CD3	/SINT	IS	RS-232: /CD, IN-LINE : /P1
44	BRK3	GND	IS	GND
45	TRNEMP3	GND	IS	GND
46	RCVRDY3	GND	IS	GND
47	TRNRDY3	GND	IS	GND
48	/CTS3	GND	IS	GND
49	RCVDT3	GND	IS	GND
50	/CI3	GND	IS	GND
51	/CS3	/SRCS	O	RS-232/INLINE chip select signal
52	D0	D0	IO	Data bus (CPU)
53	D1	D1	IO	Data bus (CPU)
54	D2	D2	IO	Data bus (CPU)
55	D3	D3	IO	Data bus (CPU)
56	GND	GND		GND
57	D4	D4	IO	Data bus (CPU)
58	D5	D5	IO	Data bus (CPU)
59	D6	D6	IO	Data bus (CPU)
60	D7	D7	IO	Data bus (CPU)
61	GND	GND		GND
62	VCC	VCC		+5V
63	X1	NC	O OSI14	NC
64	X2	#	I OSI14	System clock
65	XOUT	CLK_USART	O	Clock (USART)
66	TRCK	NC	O	NC
67	AB0	AH0	O	Address bus for USART
68	AB1	AH1	O	Address bus for USART
69	US1CH	GND	IS	GND
70	PX	NC	O	NC
71	/POF	/POFF	IS	POFF signal
72	/RSRQ	/IRQ1	3S	RS232 INTERRUPT
73	/TRV	GND	IS	GND
74	RXDATA0	NC	O	NC
75	TXE	/SRESET	O	INLINE TRNS ENABLE
76	/TRRQ	/TRQ2	3S	INLINE INTERRUPT
77	/TRQ1	/TRQ1	ON6	TIMER INTERRUPT (RS232)
78	/TRQ2	NC	ON6	TIMER INTERRUPT (INLINE)
79	A0	A0	I	Address bus for CPU
80	A1	A1	I	Address bus for CPU
81	A2	A2	I	Address bus for CPU
82	A3	A3	I	Address bus for CPU
83	A4	A4	I	Address bus for CPU
84	A5	A5	I	Address bus for CPU
85	/OPTCS	/OPTCS	I	Option chip select (from MPCA)
86	/RD	/RDO	I	Read signal (from CPU)
87	/WR	/WRO	I	Write signal (from CPU)
88	/RES	/RES	IS	Reset signal (from CPU)

Pin NO.	Name	UP-3301	I/O	Description
89	DB0	DB0	IO	DATA BUS (USART)
90	DB1	DB1	IO	DATA BUS (USART)
91	DB2	DB2	IO	DATA BUS (USART)
92	DB3	DB3	IO	DATA BUS (USART)
93	GND	GND		GND
94	DB4	DB4	IO	DATA BUS (USART)
95	DB5	DB5	IO	DATA BUS (USART)
96	DB6	DB6	IO	DATA BUS (USART)
97	DB7	DB7	IO	DATA BUS (USART)
98	/R	/RDH	O	Read signal (to USART)
99	/W	/WRH	O	Write signal (to USART)
100	VCC	VCC		+5V
101	GND	GND		GND
102	RES	RES USART	O	Reset signal (to USART)
103	TRNCLK	GND	I	GND
104	RCVCLK	GND	I	GND
105	DBTST	/SRCS	ID	RS-232/INLINE USART chip select
106	UTST	VCC	ID	+5V
107	/CSA	/CS1	IS	USART_A chip select
108	TRNDTA	TXD1	O	RS-232 transmission data signal
109	/DTRA	/DTR1	O	RS-232 data terminal ready signal
110	/RTSA	NC	O	NC
111	RCVDTA	RCVDT1	IS	RS-232 reception data signal
112	/CTSA	GND	IS	GND
113	/DSRA	/DSR1	IS	RS-232 data set ready signal
114	TRNRDYA	TRNRDY1	O	RS-232 data transmission enable signal
115	RCVRDYA	RCVRDY1	O	RS-232 data reception enable signal
116	TRNEMPA	TRNEMP1	O	RS-232 transmission buffer empty signal
117	SYCBKA	BRK1	IO	Break code detection signal
118	GND	GND		GND
119	/CSB	/CS2	IS	USART_B chip select
120	TRNDTB	TXD2	O	RS-232 transmission data signal
121	/DTRB	/DTR2	O	RS-232 data terminal ready signal
122	/RTSB	NC	O	NC
123	RCVDTB	RCVDT2	IS	RS-232 reception data signal
124	/CTSB	GND	IS	GND
125	/DSRB	/DSR2	IS	RS-232 data set ready signal
126	TRNRDYB	TRNRDY2	O	RS-232 data transmission enable signal
127	RCVRDYB	RCVRDY2	O	RS-232 data reception enable signal
128	TRNEMPB	TRNEMP2	O	RS-232 transmission buffer empty signal
129	SYCBKB	BRK2	IO	Break code detection signal
130	GND	GND		GND
131	/CSC	/CS3	IS	USART_C chip select

Pin NO.	Name	UP-3301	I/O	Description
132	TRNDTC	TXD3	O	RS-232 transmission data signal
133	/DTRC	/DTR3	O	RS-232 data terminal ready signal
134	/RTSC	/RTS3	O	USART_C request to send
135	RCVDTC	RCVDT3	IS	RS-232 reception data signal
136	/CTSC	GND	IS	GND
137	/DSRC	/DSR3	IS	RS-232 data set ready signal
138	TRNRDYC	TRNRDY3	O	RS-232 data transmission enable signal
139	RCVRDYC	RCVRDY3	O	RS-232 data reception enable signal
140	TRNEMPC	TRNEMP3	O	RS-232 transmission buffer empty signal
141	SYCBKC	NC	IO	NC
142	VCC	VCC		+5V
143	GND	GND		GND
144	/CSD	VCC	IS	USART_D chip select
145	TRNDTD	NC	O	NC
146	/DTRD	NC	O	NC
147	/RTSD	NC	O	NC
148	RCVDTD	GND	IS	GND
149	/CTSD	GND	IS	GND
150	/DSRD	GND	IS	GND
151	TRNRDYD	NC	O	NC
152	RCVRDYD	NC	O	NC
153	TRNEMPD	NC	O	NC
154	SYCBKD	NC	IO	NC
155	/WIN	/WRH	I	Write signal
156	/RIN	/RDH	I	Read signal
157	RSLCT0	AH0	I	Address bus
158	RSLCT1	AH1	I	Address bus
159	RST	RES USART	IS	Reset signal
160	MCLK	CLK USART	I,	

I TTL input

ID TTL input with pull down

IS TTL Schmidt input

ISU TTL Schmidt input with pull up

IO TTL I/O

3S 3-state Buffer (6mA)

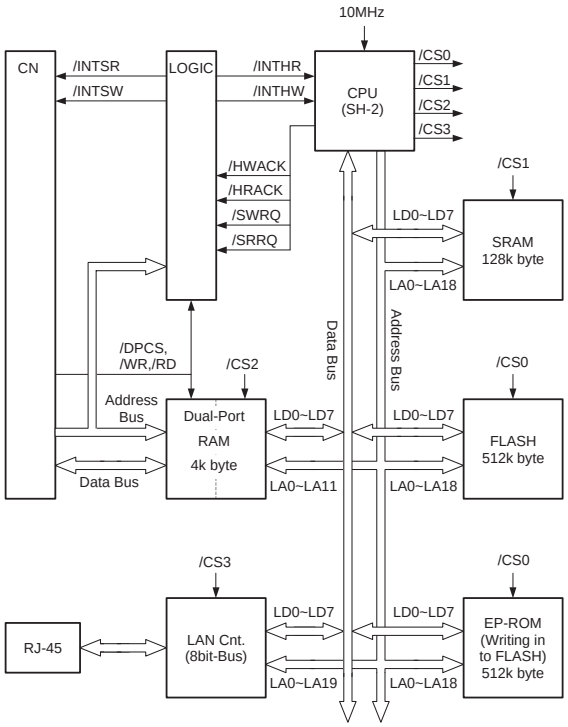
ON6 Open drain (6mA)

2-4. TCP/IP Interface

1. GENERAL DESCRIPTION

The Ethernet control supports the TCP/IP protocol.

2. BLOCK DIAGRAM



∗When writing data into FLASH, switch /CS0to EP-ROM and /CS3 to FLASH Memory.

3. CONFIGURATION

① CPU : [HitachiSH-2 Series SH7014 (20MHz)]

External memory spaces, CS0 - CS3 and the DRAM space are provided. This board assigns FLASH Memory to CS0, SRAM to CS1, dual-port SRAM to CS2, and LAN controller to CS3.

② LAN Controller : [RealtekRTL8019AS (20MHz)]

The LAN controller is assigned to the CS space.
Because of the pseudo ISA connection, each register is assigned to addresses of H00C00300 and after.

③ ROM (FLASH Memory) : [SharpLH28F004BVT(4Mbits)] <Access Time = 90ns>

The ROM (FLASH Memory) is assigned to CS0 space.
Data is written onto FLASH Memory from UV-EPROM by switching the CSO space to UV-EPROM and the CS3 space to FALSH Memory.

The MAC Address is written on FLASH Memory.

- The company code is assigned to “08001FH”.
- The serial number and adjustment byte are stored in an area of 4 bytes from the address H’0007C000.

④ RAM : [S-RAM 1Mbits] <Access Time=70ns>

Assigned to the CS1 space.

[IDT Dual-Port SRAM IDT7134] <Access Time=55ns>

Assigned to the CS2 space.

The IDT7134 does not have any busy signal, access to the same address from both sides is inhibited.

⑤ Pulse Trans : [Pulse78Z034]

Is used for the 10Base-T standard and has a choke coil built in at the output side.

4. MAIN LSI DESCRIPTION

1) CPU (SH7014)

1)-1. SH7014 Overview

The SH7014 CMOS single-chip microprocessors integrate a Hitachi-original architecture, with a high-speed CPU with peripheral functions required for the system configuration.

The CPU has a RISC-type instruction set. Most instructions can be executed in one clock cycle, which greatly improves instruction execution speed. In addition, the 32-bit internal-bus architecture enhances data processing power. With this CPU, it has become possible to assemble low cost, high performance/high-functioning systems, even for applications that were previously impossible with microprocessors, such as real-time control, which demands high speeds. In particular, the SH7040 series has a 1-kbyte on-chip cache, which allows an improvement in CPU performance during external memory access.

In addition, this LSI includes on-chip peripheral functions necessary for system configuration, such as large-capacity ROM (except the SH7014, which is ROMless) and RAM, timers, a serial communication interface (SCI), an A/D converter, an interrupt controller, and I/O ports. Memory or peripheral LSIs can be connected efficiently with an external memory access support function.

This greatly reduces system cost.

1)-1-1. SH7014 Features

CPU:

- Original Hitachi architecture
- 32-bit internal data bus
- General-register machine
  - Sixteen 32-bit general registers
  - Three 32-bit control registers
  - Four 32-bit system registers
- RISC-type instruction set
  - Instruction length: 16-bit fixed length for improved code efficiency
  - Load-store architecture (basic operations are executed between registers)
  - Delayed branch instructions reduce pipeline disruption during branch
  - Instruction set based on C language
- Instruction execution time: one instruction/cycle (35 ns/instruction at 28.7-MHz operation)
- Address space: Architecture supports 4 Gbytes
- On-chip multiplier: multiplication operations (32 bits x 32 bits → 64 bits) and multiplication/accumulation operations (32 bits x 32 bits + 64 bits → 64 bits) executed in two to four cycles
- Five-stage pipeline

Cache Memory:

- 1-kbyte instruction cache
- Caching of instruction codes and PC relative read data
- 4-byte line length (1 longword: 2 instruction lengths)
- 256 entry cache tags
- Direct map method
- On-chip RAM, and on-chip I/O areas (not related to objects of cache)
- Used in common with the on-chip RAM; 2 kbytes of on-chip RAM used as address array/data array when cache is enabled

Interrupt Controller (INTC):

- Seven external interrupt pins (NMI, $\overline{IRQ}$ x 6)
- Twenty-eight internal interrupt sources
- Sixteen programmable priority levels

Bus State Controller (BSC):

- Supports external extended memory access
  - 8-bit, or 16-bit external data bus
- Memory address space divided into five areas (four areas of SRAM space, one area of DRAM space) with the following settable features:
  - Number of wait cycles
  - Outputs chip-select signals for each area
  - During DRAM space access:
    - Outputs $\overline{RAS}$ and $\overline{CAS}$ signals for DRAM
    - Can generate a RAS precharge time assurance Tp cycle
- DRAM burst access function
  - Supports high-speed access mode for DRAM
- DRAM refresh function
  - Programmable refresh interval
  - Supports CAS-before-RAS refresh and self-refresh modes
- Wait cycles can be inserted using an external WAIT signal
- Address data multiplex I/O devices can be accessed

Note: No bus release

Direct Memory Access Controller (DMAC) (2 Channels):

- Supports cycle-steal and burst transfers
- Supports single address mode and dual address mode transfers
- Priority order: fixed at channel 0 > channel 1
- Transfer counter: 16 bits
- Transfer request sources: external DREQ input, auto-request, and on-chip supporting modules
- Address space: 4 Gbytes
- Choice of 8-, 16-, or 32-bit transfer data size

Multifunction Timer/Pulse Unit (MTU) (3 Channels):

- Maximum 8 types of waveform output or maximum 16 types of pulse I/O processing possible based on 16-bit timer, 3 channels
- 8 dual-use output compare/input capture registers
- 8 independent comparators
- 8 types of counter input clock
- Input capture function
- Pulse output mode
  - One shot, toggle, PWM
- Phase calculation mode
  - 2-phase encoder calculation processing

Compare Match Timer (CMT) (Two Channels):

- 16-bit free-running counter
- One compare register
- Generates an interrupt request upon compare match

Watchdog Timer (WDT) (One Channel):

- Watchdog timer or interval timer
- A count overflow can generate an internal reset, external signal, or interrupt

Serial Communication Interface (SCI) (Two Channels): (Per Channel):

- Asynchronous or clock-synchronous mode is selectable
- Can transmit and receive simultaneously (full duplex)
- On-chip dedicated baud rate generator
- Multiprocessor communication function

I/O Ports:

- SH7014
  - Input/output: 35
  - Input: 8
  - Total: 43

A/D Converter:

- 10 bits 8 channels
- The SH7014 has a high-speed A/D converter.

On-Chip Memory:

- ROM
  - SH7014: ROMless
- RAM: SH7014: 3 kbytes (1 kbyte when cache is used)

Operating Modes:

- Operating modes
  - Non-extended ROM mode
- Processing states
  - Program execution state
  - Exception processing state
- Power-down modes
  - Sleep mode
  - Software standby mode

Clock Pulse Generator (CPG):

- On-chip clock pulse generator
  - On-chip clock-doubling PLL circuit

1)-2. Block Diagram

Figure 1. is a block diagram of the SH7014.

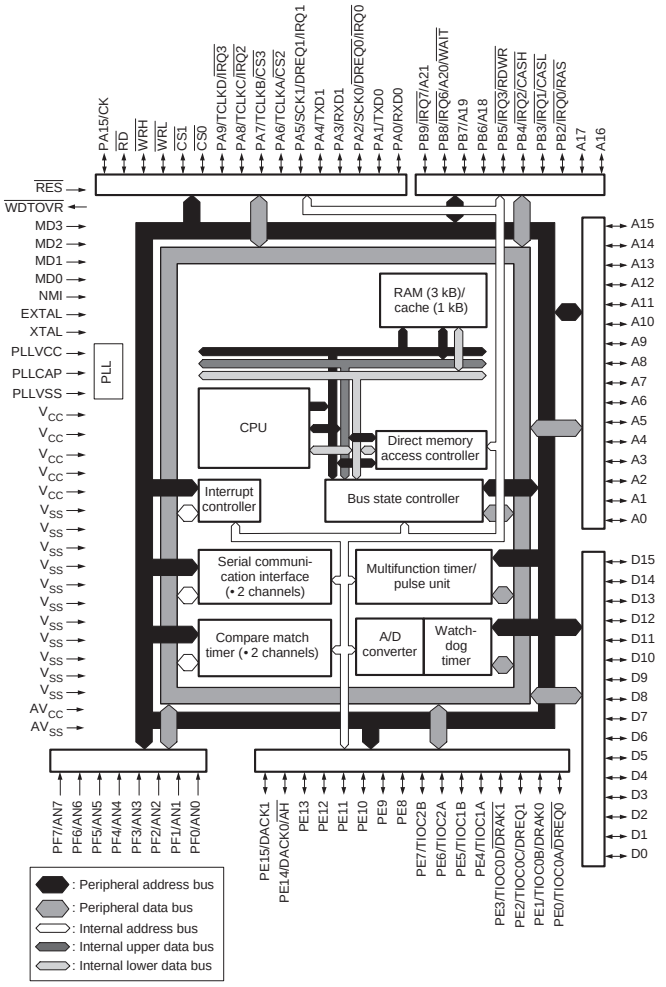


Figure 1. Block Diagram of the SH7014

1)-3. Pin Arrangement and Pin Functions

1)-3-1. Pin Arrangment

Figure 2. shows the pin arrangement for the SH7014 (top view).

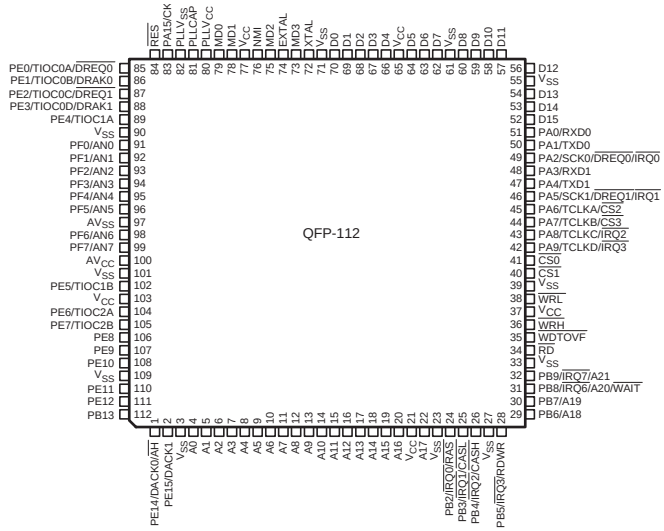


Figure 2. SH7014 Pin Arrangement (QFP-112 Top View)

CPU

No.	CPU	Signal name	I/O	Remarks
1	PE14	PE14	I	N.U. (GND)
2	PE15	/WP	I	FLASH write Status
3	Vss	GND		
4	A0	LA0	O	Address Bus
5	A1	LA1	O	
6	A2	LA2	O	
7	A3	LA3	O	
8	A4	LA4	O	
9	A5	LA5	O	
10	A6	LA6	O	
11	A7	LA7	O	
12	A8	LA8	O	
13	A9	LA9	O	
14	A10	LA10	O	
15	A11	LA11	O	
16	A12	LA12	O	
17	A13	LA13	O	
18	A14	LA14	O	
19	A15	LA15	O	
20	A16	LA16	O	
21	Vcc	+5V		
22	A17	LA17	O	Address Bus
23	Vss	GND		
24	/IRQ0	/INTHW	I	Host write end interrupt
25	/IRQ1	/INTHR	I	Host write end interrupt
26	/IRQ2	/INTLAN	I	Interrupt from LANC
27	Vss	GND		
28	/IRQ3	/IRQ3	I	N.U. (+5V)
29	A18	LA18	O	Address Bus
30	A19	LA19	O	Address Bus
31	/WAIT	IOCHRDY	I	Wait from LANC
32	PB9	PB9	I	N.U. (GND)
33	Vss	GND		
34	/RD	/MRD	O	Memory Read
35	/WDTOVF	/WDTOVF	O	N.U. (OPEN)
36	/WRH	/WRH	O	N.U. (OPEN)
37	Vcc	+5V		
38	/WRL	/MWE	O	Memory Write
39	Vss	GND		
40	/CS1	/CS1	O	SRAM Chip Select
41	/CS0	/CS0	O	FLASH Chip Select
42	PA9	PA9	I	N.U. (GND)
43	PA8	PA8	I	N.U. (GND)
44	/CS3	/CS3	O	LANC Chip Select
45	/CS2	/CS2	O	DP-RAM Chip Select
46	PA5	PA5	I	N.U. (GND)
47	PA4	PA4	I	N.U. (GND)
48	PA3	PA3	I	N.U. (GND)
49	PA2	PA2	I	N.U. (GND)
50	PA1	PA1	I	N.U. (GND)
51	PA0	PA0	I	N.U. (GND)
52	D15	HD15	I/O	N.U. (Pull-Down)
53	D14	HD14	I/O	N.U. (Pull-Down)
54	D13	HD13	I/O	N.U. (Pull-Down)
55	Vss	GND		
56	D12	HD12	I/O	N.U. (Pull-Down)
57	D11	HD11	I/O	N.U. (Pull-Down)
58	D10	HD10	I/O	N.U. (Pull-Down)
59	D9	HD9	I/O	N.U. (Pull-Down)
60	D8	HD8	I/O	N.U. (Pull-Down)
61	Vss	GND		
62	D7	HD7	I/O	DATA Bus
63	D6	HD6	I/O	
64	D5	HD5	I/O	
65	Vcc	+5V		
66	D4	HD4	I/O	DATA Bus
67	D3	HD3	I/O	
68	D2	HD2	I/O	
69	D1	HD1	I/O	
70	D0	HD0	I/O	
s71	Vss	GND		
72	XTAL	XTAL	O	Oscillator connection terminal
73	MD3	MD3	I	Mode terminal
74	EXTAL	EXTAL	I	Oscillator connection terminal
75	MD2	MD2	I	Mode terminal 2
76	NMI	NMI	I	N.U. (+5V)
77	Vcc	+5V		
78	MD1	MD1	I	Mode terminal 1
79	MD0	MD0	I	Mode terminal 0
80	PLLVcc	PLLVcc		
81	PLLCAP	PLLCAP		
82	PLLVss	PLLVss		
83	PA15	PA15	I	N.U.(Pull-Down)
84	/RES	/LRES	I	Hardware Reset
85	PE0	PE0	I	N.U. (GND)
86	PE1	PE1	I	N.U. (GND)
87	PE2	PE2	I	N.U. (GND)
88	PE3	PE3	I	N.U. (GND)
89	PE4	PE4	I	N.U. (GND)
90	Vss	GND		
91	PF0	PF0	I	N.U. (GND)
92	PF1	PF1	I	N.U. (GND)
93	PF2	PF2	I	N.U. (GND)
94	PF3	PF3	I	N.U. (GND)
95	PF4	PF4	I	N.U. (GND)
96	PF5	PF5	I	N.U. (GND)
97	AVss	GND		
98	PF6	PF6	I	N.U. (GND)
99	PF7	PF7	I	N.U. (GND)
100	AVcc	+5V		
101	Vss	GND		
102	PE5	PE5	I	N.U. (GND)
103	Vcc	+5V		
104	PE6	PE6	I	N.U. (GND)
105	PE7	PE7	I	N.U. (GND)
106	PE8	/SRRQ	O	Slave read end request
107	PE9	/SWRQ	O	Slave write end request
108	PE10	/HRACK	O	Host read interrupt cancel
109	Vss	GND		
110	PE11	/HWACK	O	Host write interrupt cancel
111	PE12	PE12	O	N.U. (OPEN)
112	PE13	/RSTDRV	O	Soft Reset for LANC

Note: Signals prefixed with a slash "/" are active in low level.

2) LAN CONTROLLER (RTL8019AS)

2)-1. Features:

- 100-pin PQFP
- Supports PnP auto detect mode
- Compliant to Ethernet II and IEEE802.3 10Base5, 10Base2, 10BaseT
- Software compatible with NE2000 on both 8 and 16-bit slots
- Supports both jumper and jumperless modes
- Supports Microsofts Plug and Play configuration for jumperless mode
- Supports Full-Duplex Ethernet function to double channel bandwidth
- Supports three level power down modes:
  - – Sleep
  - – Power down with internal clock running
  - – Power down with internal clock halted
- Built-in data prefetch function to improve performance
- Supports UTP, AUI & BNC auto-detect
- Supports auto polarity correction for 10BaseT
- Supports 8 IRQ lines
- Supports 16 I/O base address options

  --- and extra I/O address fully decode mode
- Supports 16K, 32K, 64K and 16K-page mode access to BROM (up to 256 pages with 16K bytes/page)
- Supports BROM disable command to release memory after remote boot
- Supports flash memory read/write
- 16k byte SRAM built in
- Uses a 9346 (64*16-bit EEPROM) to store resource configurations and ID parameters
- Capable of programming blank 9346 on board for manufacturing convenience
- Support 4 diagnostic LED pins with programmable outputs

2)-2. General Description

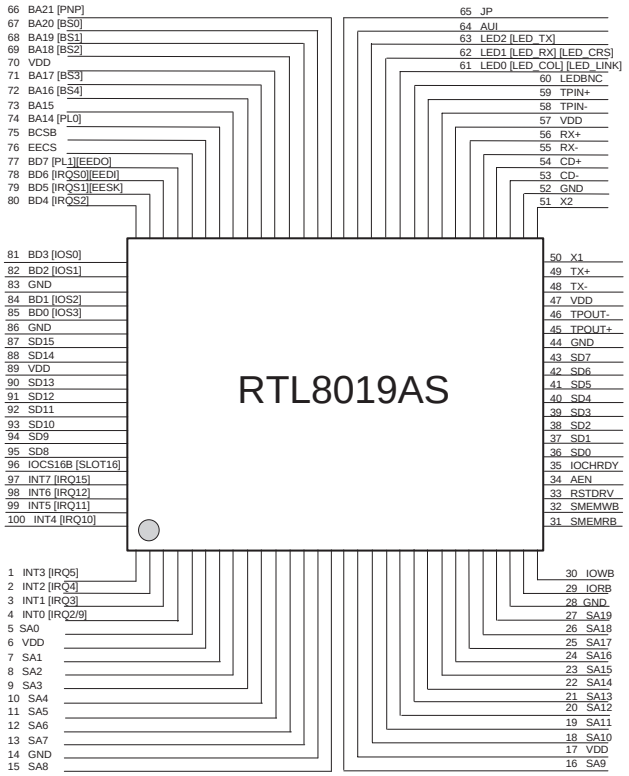
The RTL8019AS is a highly integrated Ethernet Controller which offers a simple solution to implement a Plug and Play NE2000 compatible adapter with full-duplex and power down features.

With the three level power down control features, the RTL8019AS is made to be an ideal choice of the network device for a GREEN PC system. The full-duplex function enables simultaneously transmission and reception on the twisted-pair link to a full-duplex Ethernet switching hub. This feature not only increases the channel bandwidth from 10 to 20 Mbps but also avoids the performance degrading problem due to the channel contention characteristics of the Ethernet CSMA/CD protocol.

The RTL8019AS provides the auto-detect capability between the integrated 10BaseT transceiver, BNC and AUI interface. Besides, the 10BaseT transceiver can automatically correct the polarity error on its receiving pair.

The RTL8019AS is built in with a 16K-byte SRAM in a single chip. It is designed not only to provide more friendly functions but also to save the effort of SRAM sourcing and inventory.

2)-3. Pin Configuration



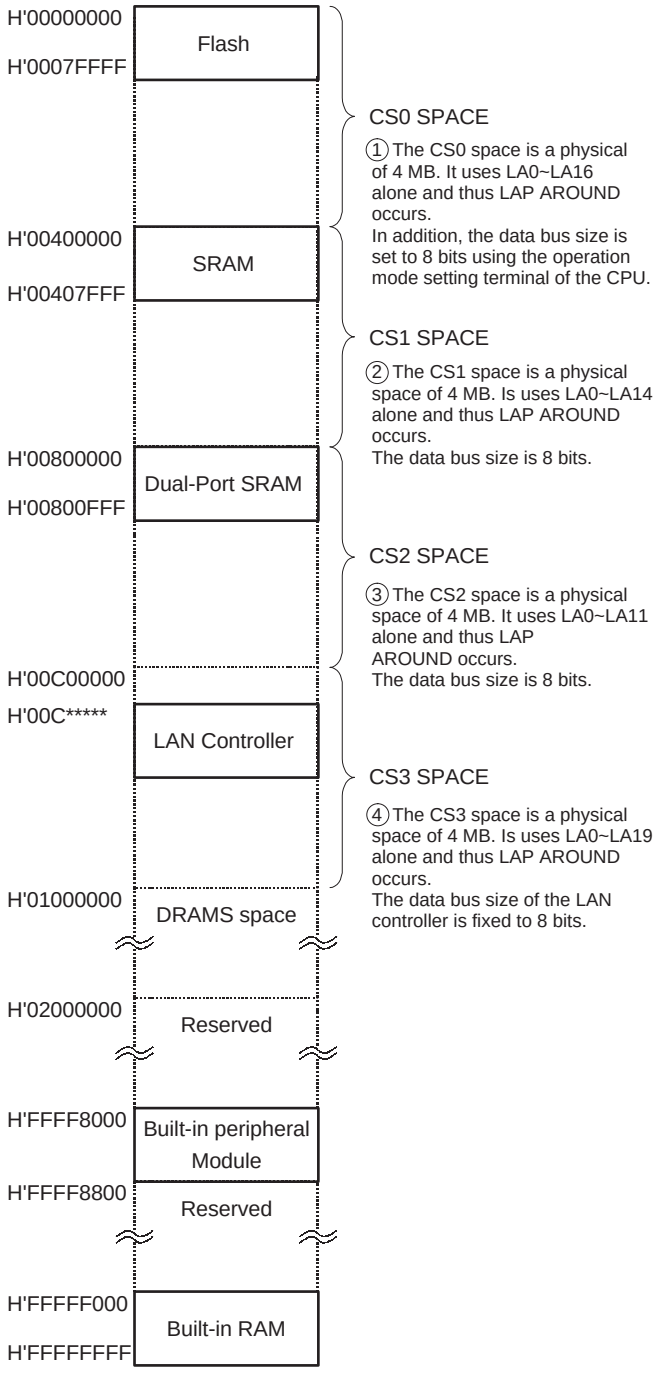
LAN Controller

No.	CPU	Signal name	I/O	Remarks
1	INT3	INT3	O	N.U. (Pull-Down)
2	INT2	INT2	O	N.U. (Pull-Down)
3	INT1	INT1	O	N.U. (Pull-Down)
4	INT0	/INTLAN	O	Interrupt to CPU
5	SA0	LA0	I	Address Bus
6	VDD	+5V		
7	SA1	LA1	I	Address Bus
8	SA2	LA2	I	
9	SA3	LA3	I	
10	SA4	LA4	I	
11	SA5	LA5	I	
12	SA6	LA6	I	
13	SA7	LA7	I	
14	GND	GND		
15	SA8	LA8	I	Address Bus
16	SA9	LA9	I	
17	VDD	+5V		
18	SA10	LA10	I	Address Bus
19	SA11	LA11	I	
20	SA12	LA12	I	
21	SA13	LA13	I	
22	SA14	LA14	I	
23	SA15	LA15	I	
24	SA16	LA16	I	
25	SA17	LA17	I	
26	SA18	LA18	I	
27	SA19	LA19	I	
28	GND	GND		
29	IORB	/MRD	I	Memory Read
30	IOWB	/MWE	I	Memory Write
31	SMEMRB	SMEMRB	I	N.U. (Pull-Up)

No.	CPU	Signal name	I/O	Remarks
32	SMEMWB	SMEMWB	I	N.U. (Pull-Up)
33	RSTDRV	RSTDRV	I	Hardware Reset
34	AEN	/CS3	I	Chip Select
35	IOCHRDY	/WAIT	O	Wait to CPU
36	SD0	LD0	I/O	DATA Bus
37	SD1	LD1	I/O	
38	SD2	LD2	I/O	
39	SD3	LD3	I/O	
40	SD4	LD4	I/O	
41	SD5	LD5	I/O	
42	SD6	LD6	I/O	
43	SD7	LD7	I/O	
44	GND	GND		
45	TPOUT+	TPOUT+	O	10Base-T output +
46	TPOUT-	TPOUT-	O	10Base-T output -
47	VDD	+5V		
48	TX-	TX-	O	N.U. (Pull-Down)
49	TX+	TX+	O	N.U. (Pull-Down)
50	X1	X1	I	Oscillator connection terminal
51	X2	X2	O	Oscillator connection terminal
52	GND	GND		
53	CD-	CD-	I	N.U. (OPEN)
54	CD+	CD+	I	N.U. (OPEN)
55	RX-	RX-	I	N.U. (OPEN)
56	RX+	RX+	I	N.U. (OPEN)
57	VDD	+5V		
58	TPN-	TPIN-	I	10Base-T input -
59	TPN+	TPIN+	I	10Base-T input +
60	LEDBNC	LEDBNC	O	N.U. (OPEN)
61	LED0	LED0	O	N.U. (OPEN)
62	LED1	LED1	O	N.U. (OPEN)
63	LED2	LED2	O	N.U. (OPEN)
64	AUI	AUI	I	GND
65	JP	JP	I	Pull-Up
66	PNP	PNP	I	OPEN
67	BS0	BS0	I	OPEN
68	BS1	BS1	I	OPEN
69	BS2	BS2	I	OPEN
70	VDD	+5V		
71	BS3	BS3	I	OPEN
72	BS4	BS4	I	OPEN
73	BA15	BA15	O	N.U. (OPEN)
74	PL0	PL0	I	OPEN
75	BCSB	BCSB	O	N.U. (OPEN)
76	EECS	EECS	O	N.U. (OPEN)
77	PL1	PL1	I	OPEN
78	IRQS0	IRQS0	I	OPEN
79	IRQS1	IRQS1	I	OPEN
80	IRQS2	IRQS2	I	OPEN
81	IOS0	IOS0	I	OPEN
82	IOS1	IOS1	I	OPEN
83	GND	GND		
84	IOS2	IOS2	I	OPEN
85	IOS3	IOS3	I	OPEN
86	GND	GND		
87	SD15	SD15	I/O	N.U. (Pull-Down)
88	SD14	SD14	I/O	N.U. (Pull-Down)
89	VDD	+5V		
90	SD13	SD13	I/O	N.U. (Pull-Down)
91	SD12	SD12	I/O	N.U. (Pull-Down)
92	SD11	SD11	I/O	N.U. (Pull-Down)
93	SD10	SD10	I/O	N.U. (Pull-Down)
94	SD9	SD9	I/O	N.U. (Pull-Down)
95	SD8	SD8	I/O	N.U. (Pull-Down)
96	SLOT16	SLOT16	I	Pull-Down
97	INT7	INT7	O	N.U. (Pull-Down)
98	INT6	INT6	O	N.U. (Pull-Down)
99	INT5	INT5	O	N.U. (Pull-Down)
100	INT4	INT4	O	N.U. (Pull-Down)

Note: Signals suffixed with the letter “B” are active in low level.

5. MEMORY MAP


H'00000000
Flash
H'0007FFFF
CS0 SPACE
① The CS0 space is a physical of 4 MB. It uses LA0~LA16 alone and thus LAP AROUND occurs.
In addition, the data bus size is set to 8 bits using the operation mode setting terminal of the CPU.
H'00400000
SRAM
H'00407FFF
CS1 SPACE
② The CS1 space is a physical space of 4 MB. Is uses LA0~LA14 alone and thus LAP AROUND occurs.
The data bus size is 8 bits.
H'00800000
Dual-Port SRAM
H'00800FFF
CS2 SPACE
③ The CS2 space is a physical space of 4 MB. It uses LA0~LA11 alone and thus LAP AROUND occurs.
The data bus size is 8 bits.
H'00C00000
H'00C*****
LAN Controller
CS3 SPACE
④ The CS3 space is a physical space of 4 MB. Is uses LA0~LA19 alone and thus LAP AROUND occurs.
The data bus size of the LAN controller is fixed to 8 bits.
H'01000000
DRAMS space
H'02000000
Reserved
H'FFFF8000
Built-in peripheral Module
H'FFFF8800
Reserved
H'FFFFF000
Built-in RAM
H'FFFFFFFF

6. INTERFACE WITH HOST CPU

1) SIGNAL LINES

The following signal lines are required for the interface with the host CPU.

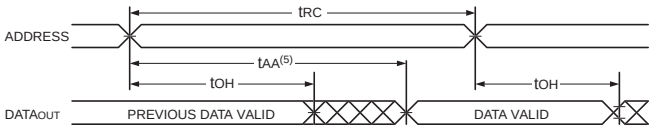
Signal name	I/O	Description	Connected to	Connection pin
A0~A11	I	Address Bus from host CPU	DP-RAM	A0R~A11R
D0~D7	I/O	Data Bus from host CPU	DP-RAM	D0R~D7R
/RD	I	Read signal from host CPU	DP-RAM	/OER
/WR	I	Write signal from host CPU	DP-RAM	R/WR
/DPCS	I	Chip select from host CPU	DP-RAM	/CER
/LRES	I	Rest signal for this board from host CPU	Board CPU	/RES
/INTSR	O	Data read end interrupt from board CPU	LOGIC	
/INTSW	O	Data write end interrupt from board CPU	LOGIC	
A13~A15	I	Address bus from host CPU (for decode)	LOGIC	
Vcc		Power (+5V)		
GND		GND	,	

Note: Signals prefixed with a slash "/" are active in low level.

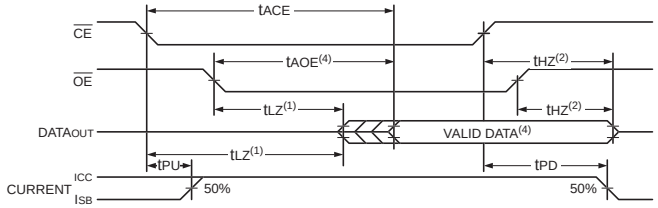
Cautions to be taken when designing the host side

1. It is preferable that /LRES signal to be input into the board can also be controlled by software.
2. The access timing satisfies the dual-port SRAM specification.

• Timing Waveform of Read Cycle No. 1, Either Side (1,2,4)



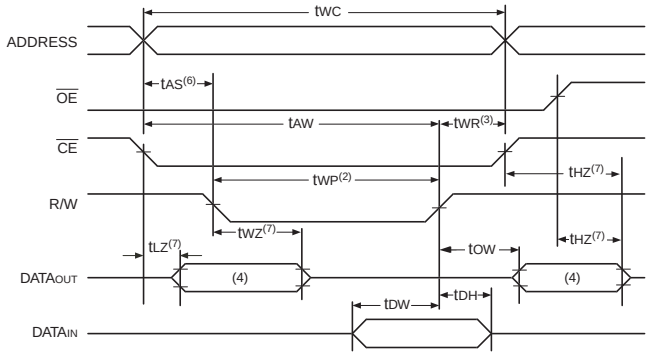
• Timing Waveform of Read Cycle No. 2, Either Side (1,3)



NOTES:

1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/W = VIH.
4. The start of valid data depends on which timing becomes effective, tAOE, tACE or tAA
5. tAA is for RAM Address Access and tSAA for is Semaphore Address Access.

• Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing (1,5,8)



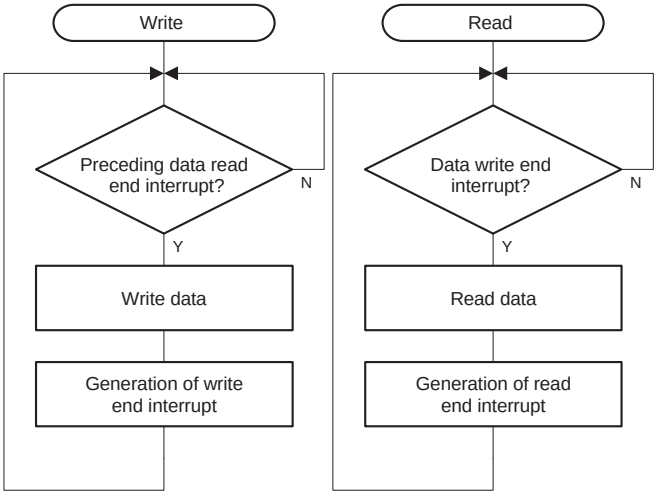
NOTES:

1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a $\overline{CE}$ =VIL and R/$\overline{W}$ = VIL.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going to VIH to the end-of-write cycle.
4. During this period, the I/O pins are in the output state, and the input signals must not be applied.
5. If the $\overline{CE}$ = VIL transition occurs simultaneously with or after the R/$\overline{W}$ = VIL transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ±500mV from the steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ = VIL during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ = VIH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

2) DATA COMMUNICATION

Data is transmitted from the host CPU to the TCP/IP board or vice versa through the dual-port SRAM. If data is written into the same address of the dual-port SRAM from both sides or written into and read from the same address from both sides, data is not assured. The following procedure should be observed.

The format of data to be handled should meet the software specifications.



- Interrupt signals from the host to board : Write/INTHW (Host Write), Read/INTHR (Host Read)

  /INTHW (Host Write) is generated by writing into the address H'7*** of the dual-port SRAM and cancelled by outputting the /HWACK signal by 100ns LOW pulse.

  /INTHR (Host Read) is generated by reading the address H'B*** of the dual-port SRAM and cancelled by outputting the /HRACK signal by 100ns LOW pulse.

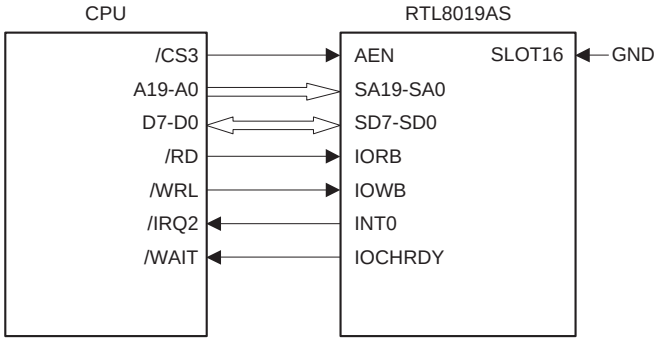
- Interrupt signals from the board to host : Write /INTSW (Slave Write), Read /INTSR (Slave Read)

  /INTSW (Slave Write) is generated by outputting the /SWRQ signal by 100ns LOW pulse and cancelled by writing data into the address H'B*** of the dual-port SRAM from the host side.

  /INTSR (Slave Read) is generated by outputting the /SRRQ signal by 100ns low pulse and cancelled by reading data from the address H'7*** of the dual-port SRAM.

7. LAN CONTROL

This board fixes RTL8019AS to the 8-bit mode on hardware.



The initial values of the items in the table are set as shown below by hardware.

Item	Setting	Remarks
I/O Base Address	300H	IOS3~0=0,0,0,0
Network Media Type	TP/CX automatic detection	PL1~0=0,0
BROM Size & Memory Base Address	Disable	BS4~0=0,0,0,0,0
IRQ Select	INT0	IRQS2~0=0,0,0

Any data loading EEPROM is not used. MAC address is written by the CPU reading data on the flash memory and writing the register to the LAN controller.

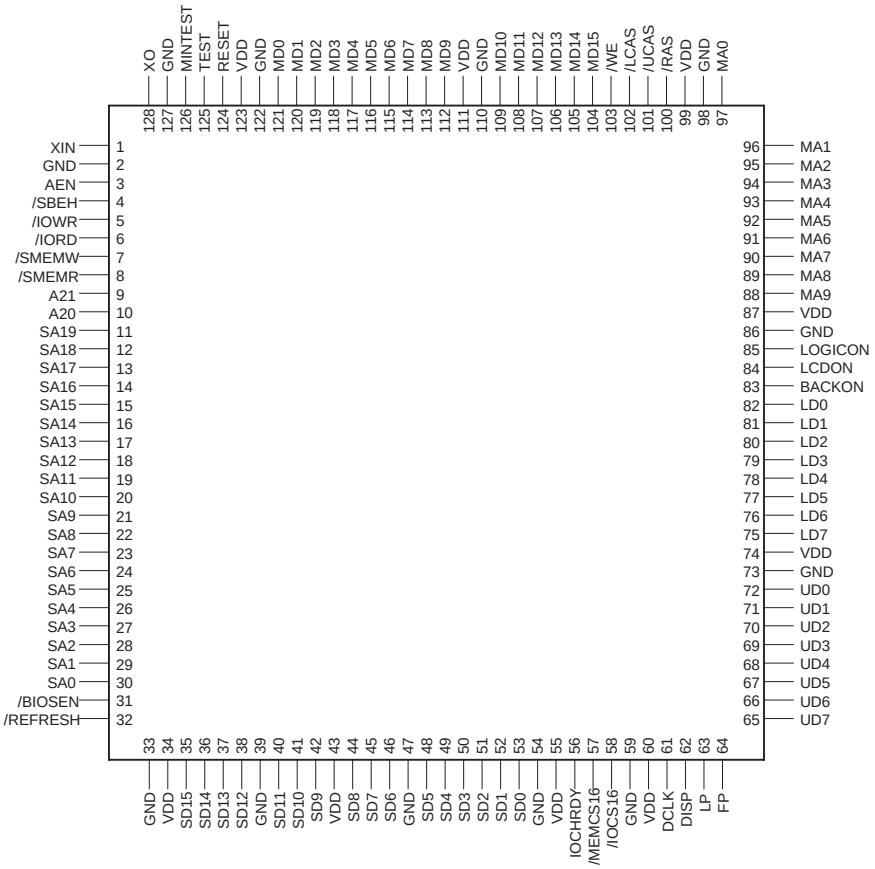
8. PORT SETTING

① The common pins of the CPU are set as shown below.

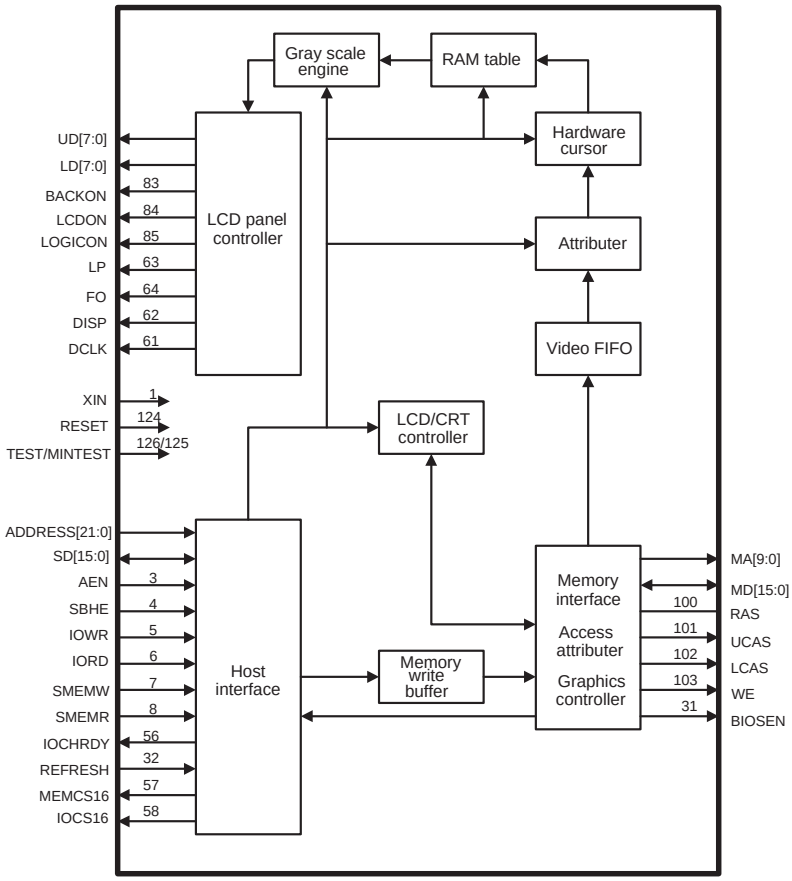
Pin No	I/O	Selection signal	Remarks
2	I	PE15	/WP(FLASH write STATUS)
24	I	/IRQ0	Host write end interrupt (↓ Edge detection)
25	I	/IRQ1	Host read end interrupt (↓ Edge detection)
26	I	/IRQ2	Interrupt from LANC (↓ Edge detection)
28	I	/IRQ3	Reserve (↓ Edge detection)
29	O	A18	Address Bus
30	O	A19	Address Bus
31	I	/WAIT	wait from LANC
44	O	/CS3	Chip Select for LAN (Usual access space)
45	O	/CS2	Chip Select for dual-port SRAM
106	O	PE8	/SRRQ (Board side read end request)
107	O	PE9	/SWRQ (Board side write end request)
108	O	PE10	/HRACK (host side read end interrupt cancel)
110	O	PE11	/HWACK (host side write end interrupt cancel)
112	O	PE13	/RSTDRViActive Lowj

2-5. VGA controller (MN89303A)

1) Pin Configuration



2) Block diagram



3) Pin configuration

Pin No.	Symbol	Signal name	In/Out	Function
1	XIN	XIN	In	25.175MHz
2	GND	GND	In	GND
3	AEN	GND	In	GND
4	/SBEH	/SBEH	In	System byte high enable
5	/IOWR	/IOWR	In	I/O write
6	/IORD	/IORD	In	I/O read
7	/SMEMW	/SMEMW	In	Memory write
8	/SMEMR	/SMEMR	In	Memory read
9	A21	GND	In	GND
10	A20	GND	In	GND
11	SA19	VCC	In	+5V
12	SA18	GND	In	GND
13	SA17	VCC	In	+5V
14	SA16	A16	In	Address bus
15	SA15	A15	In	Address bus
16	SA14	A14	In	Address bus
17	SA13	A13	In	Address bus
18	SA12	A12	In	Address bus
19	SA11	A11	In	Address bus
20	SA10	A10	In	Address bus
21	SA9	A9	In	Address bus
22	SA8	A8	In	Address bus
23	SA7	A7	In	Address bus
24	SA6	A6	In	Address bus
25	SA5	A5	In	Address bus
26	SA4	A4	In	Address bus
27	SA3	A3	In	Address bus
28	SA2	A2	In	Address bus
29	SA1	A1	In	Address bus
30	SA0	A0	In	Address bus
31	/BIOSEN	NC	In	NC
32	/REFRESH	/RFSH	In	Refresh signal
33	GND	GND	In	GND
34	VDD	VCC	In	+5V
35	SD15	D7	I/O	Data bus
36	SD14	D6	I/O	Data bus
37	SD13	D5	I/O	Data bus
38	SD12	D4	I/O	Data bus
39	GND	GND	In	GND
40	SD11	D3	I/O	Data bus
41	SD10	D2	I/O	Data bus
42	SD9	D1	I/O	Data bus
43	VDD	VCC	In	+5V
44	SD8	D0	I/O	Data bus
45	SD7	D15	I/O	Data bus
46	SD6	D14	I/O	Data bus
47	GND	GND	In	GND
48	SD5	D13	I/O	Data bus
49	SD4	D12	I/O	Data bus
50	SD3	D11	I/O	Data bus
51	SD2	D10	I/O	Data bus
52	SD1	D9	I/O	Data bus
53	SD0	D8	I/O	Data bus
54	GND	GND	In	GND
55	VDD	VCC	In	+5V
56	IOCHRDY	/VWAITI	Out	Channel ready signal
57	/MEMCS16	NC	In	NC
58	/IOCS16	NC	In	NC

Pin No.	Symbol	Signal name	In/Out	Function
59	GND	GND	In	GND
60	VDD	VCC	In	+5V
61	DCLK	XCK	Out	Data shift clock
62	DISP	DISP	Out	Display enable
63	LP	LP	Out	Line pulse
64	FP	YD	Out	Frame pulse
65	UD7	DU7	Out	Upper data
66	UD6	DU6	Out	Upper data
67	UD5	DU5	Out	Upper data
68	UD4	DU4	Out	Upper data
69	UD3	DU3	Out	Upper data
70	UD2	DU2	Out	Upper data
71	UD1	DU1	Out	Upper data
72	UD0	DU0	Out	Upper data
73	GND	GND	In	GND
74	VDD	VCC	In	+5V
75	LD7	DL7	Out	Lower data
76	LD6	DL6	Out	Lower data
77	LD5	DL5	Out	Lower data
78	LD4	DL4	Out	Lower data
79	LD3	DL3	Out	Lower data
80	LD2	DL2	Out	Lower data
81	LD1	DL1	Out	Lower data
82	LD0	DL0	Out	Lower data
83	BACKON	BKLT	Out	Back light On
84	LCDON	LCDON	Out	LCD drive power on signal
85	LOGICON	NC	Out	LCD logic power on signal
86	GND	GND	In	GND
87	VDD	VCC	In	+5V
88	MA9	NC	Out	NC
89	MA8	MA8	Out	Memory address bus
90	MA7	MA7	Out	Memory address bus
91	MA6	MA6	Out	Memory address bus
92	MA5	MA5	Out	Memory address bus
93	MA4	MA4	Out	Memory address bus
92	MA3	MA3	Out	Memory address bus
91	MA2	MA2	Out	Memory address bus
92	MA5	MA5	Out	Memory address bus
93	MA4	MA4	Out	Memory address bus
94	MA3	MA3	Out	Memory address bus
95	MA2	MA2	Out	Memory address bus
96	MA1	MA1	Out	Memory address bus
97	MA0	MA0	Out	Memory address bus
98	GND	GND	In	GND
99	VDD	VCC	In	VCC
100	/RAS	/RASV	Out	RAS address strobe
101	/UCAS	/UCASV	Out	Upper CAS address strobe
102	/LCAS	/LCASV	Out	Lower CAS address strobe
103	/WE	/WEV	Out	Write enable
104	MD15	MD15	I/O	Memory data
105	MD14	MD14	I/O	Memory data
106	MD13	MD13	I/O	Memory data
107	MD12	MD12	I/O	Memory data
108	MD11	MD11	I/O	Memory data
109	MD10	MD10	I/O	Memory data
110	GND	GND	In	GND
111	VDD	VCC	In	+5V
112	MD9	MD9	I/O	Memory data

Pin No.	Symbol	Signal name	In/Out	Function
113	MD8	MD8	I/O	Memory data
114	MD7	MD7	I/O	Memory data
115	MD6	MD6	I/O	Memory data
116	MD5	MD5	I/O	Memory data
117	MD4	MD4	I/O	Memory data
118	MD3	MD3	I/O	Memory data
119	MD2	MD2	I/O	Memory data
120	MD1	MD1	I/O	Memory data
121	MD0	MD0	I/O	Memory data
122	GND	GND	In	GND
123	VDD	VCC	In	+5V
124	RESET	RESET	In	Reset signal
125	MINTEST	GND	In	GND
126	TEST	GND	In	GND
127	GND	GND	In	GND
128	XO	XO	Out	25.175MHz

2-6. CKDC9 (HD404728A91FS)

1) General description

The CKDC7 is a 4-bit microcomputer developed for the UP-3301 and provides functions to control the real-time clock, keys, and displays. The basic functions of the CKDC9 are shown below.

Keys: The CKDC9 is capable of controlling a maximum of 256 momentary keys. (Sharp 2-key rollover control)
Simultaneous scanning of key and switch
(When a key is scanned, the state of a mode is buffered.)

Switches: Mode switch with 14 positions maximum
8-bit clerk (cashier) switch (not used)
2-bit feed switch
1-bit receipt on/off switch
1-bit option switch
4-bit general-purpose switch (1-bit is used for keyboard select)

Displays: 16-column dot display
12-column 7-segment display (column digit selectable)
All column blink controlled for the dot and 7-segment display decimal point and indicators
Programmable patterns for 7-segment display:
Four patterns
Internal driver for 7-segment display

Buzzer: Single tone control

Clock: Year, month, day of month, day of week, hour, minute

Alarm: Hour, minute

Interrupt request (event control):

Detection of key input, mode switch position change, alarm issue, and counter overflow

2) Pin description

Pin No.	Symbol	Signal name	In/ Out	Function
1	SB	SB	Out	Segment B
2	SC	SC	Out	Segment C
3	SD	SD	Out	Segment D
4	SE	SE	Out	Segment E
5	SF	SF	Out	Segment F
6	SG	SG	Out	Segment G
7	P4	AP	Out	
8	P0	NC	–	NC
9	P1	NC	–	NC
10	P2	DP	Out	Decimal point
11	P3	ID	Out	Indicator
12	$\overline{\text{MODR}}$	VCC	–	+5V
13	$\overline{\text{CFSR}}$	$\overline{\text{CFSR}}$	In	Clerk key, Feed key, Switch return signal
14	KEX0	NC	Out	NC
15	KEX1	NC	Out	NC
16	RQ	GND	–	GND
17	SKR0	VCC	–	+5V
18	ST0	ST0	Out	Key strobe signal
19	ST1	ST1	Out	Key strobe signal
20	ST2	ST2	Out	Key strobe signal
21	ST3	ST3	Out	Key strobe signal
22	$\overline{\text{POFF}}$	$\overline{\text{POFF}}$	In	Power off signal
23	$\overline{\text{STOP}}$	$\overline{\text{STOP}}$	In	STOP signal
24	$\overline{\text{DDIG}}$	VCC	–	+5V
25	$\overline{\text{DCS}}$	$\overline{\text{DCS}}$	–	Dot display controller chip select $\overline{\text{DCS}}$
26	VCC	$\overline{\text{VCKDC}}$	–	+5V
27	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$	In	Clock signal
28	HTS	HTS	In	Key data from host
29	STH	STH	Out	Key data to host
30	SDISP	GND	–	GND
31	BUZZ	BUZZ	Out	Buzzer
32	$\overline{\text{DSCK}}$	$\overline{\text{DSCK}}$	–	Dot display controller $\overline{\text{SCK}}$
33	$\overline{\text{SRES}}$	$\overline{\text{RESET}}$	Out	Reset signal
34	DS0	$\overline{\text{DSO}}$	–	Dot display controller SO
35	$\overline{\text{SHEN}}$	$\overline{\text{SHEN}}$	Out	Shift enable signal
36	$\overline{\text{IRQ}}$	$\overline{\text{KRQ}}$	Out	Key request signal
37	KR0	$\overline{\text{KR0}}$	In	Key return signal
38	KR1	$\overline{\text{KR1}}$	In	Key return signal
39	KR2	$\overline{\text{KR2}}$	In	Key return signal
40	KR3	$\overline{\text{KR3}}$	In	Key return signal
41	RESET	CKDCR	In	CKDC reset signal
42	OSC2	OSC2	–	Clock
43	OSC1	OSC1	–	Clock
44	GND	GND	–	GND
45	CL1	CL1	–	Time clock
46	CL2	CL2	–	Time clock
47	TEST	VCKDC	–	+5V
48	G0	G1	Out	Display digit signal
49	G1	G2	Out	Display digit signal
50	G2	G3	Out	Display digit signal
51	G3	G4	Out	Display digit signal
52	G4	G5	Out	Display digit signal
53	G5	G6	Out	Display digit signal
54	G6	G7	Out	Display digit signal
55	G7	G8	Out	Display digit signal
56	G8	G9	Out	Display digit signal
57	G9	G10	Out	Display digit signal
58	G10	G11	Out	Display digit signal
59	G11	NC	Out	NC
60	PO0	NC		NC
61	PO1	NC		NC
62	PO2	NC	–	NC
63	PO3	NC	–	NC
64	SA	SA	–	Segment A

2-6. ISP2032

This IC has been developed specifically for the UP-3301 to achieve the VGA CHIP and PSRAM interfaces.

Pin descriotion

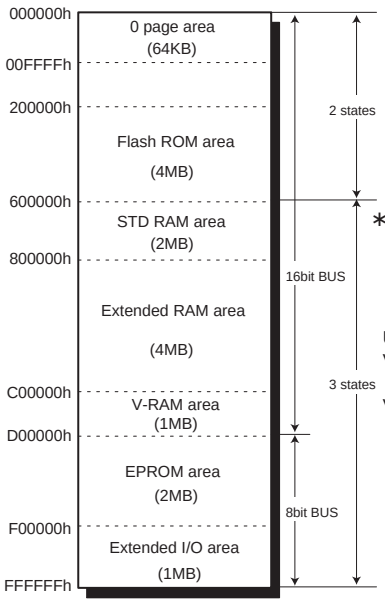
Pin No.	Name	I/O	Function
1	/VMEM	In	VIDEO MEMORY DECODE 00000H ~ C1FFFFH 16bit/8bit access, 8 bit read from the CPU is treated as 16-bit on the VGA.
2	/VMEM2	In	VIDEO MEMORY DECODE (ONLY FOR GRAPHICS MODE; 8BIT) C80000H ~ C9FFFFH 8-bit access only. /VMEM and /VMEM2 differ in their apparent address to each other, but the contents of memory to be accessed are the same. They differ in access method (WORD/BYTE).
3	/HWR	In	HIGH BYTE WRITE FROM CPU
4	/LWR	In	LOW BYTE WRITE FROM CPU
5	PHAI	In	CLOCK FROM CPU
6	VCC		
7	/ISPEN	In	for ISP (In System Program)
8	/VWAITI	In	WAIT FROM VGA CHIP (IOCHRDY)
9	/VWAIT	Out	WAIT TO MPCA There are the following ORs. ① IOCHRDY from VGA CHIP ② 1 WAIT is generated when VRAM. VGA I/O is accessed. (Because IOCHRDY is slow, 1 WAIT is generated prior to it.)
10	/DWRI	In	DELAYED WRITE (FOR VGA CHIP TIMING)
11	/DWRO	Out	WRITE FOR /DWRI
12	/DRDI	In	DELAYED READ (FOR VGA CHIP TIMING)
13	/DRD	Out	READ FOR /PRDI
14	RES	Out	RESET OUTPUT RESET ← NOT (/RESET)
15	/RES	In	/RESET INPUT
16	A0	In	A0
17	GND		
18	A20	In	A20
19	PCE21E	Out	EXTENDED PSRAM1 DECODER (EVEN) 800000H ~ 8FFFFFH
20	PCE210	Out	EXTENDED PSRAM1 DECODER (ODD) 800000H ~ 8FFFFFH
21	PCE220	Out	EXTENDED PSRAM2 DECODER (ODD) 900000H ~ 9FFFFFH
22	PCE22E	Out	EXTENDED PSRAM2 DECODER (EVEN) 900000H ~ 9FFFFFH
23	/IPLON0	In	IPL SIGNAL
24	/PSRF0	Out	PSRAM REFRESH
25	/OWR	Out	PSRAM WRITE (ODD SIDE)
26	/M3SWP	Out	MODE3 BUS SWAP (FOR PSRAM ACCESS DURING IPL)
27	Y2/SCLK		ISP
28	VCC		
29	Y1/RESET		ISP
30	MODE		ISP
31	RASPN2E	In	EXTENDED PSRAM2 DECODER (FROM MPCA) 800000H ~ 9FFFFFH
32	RASPN2	In	EXTENDED PSRAM2 DECODER (FROM MPCA) 800000H ~ 9FFFFFH
33	/RASPN12	In	PSRAM DECODER (FROM MPCA) 600000H ~ 9FFFFFH
34	/AS	In	/AS FROM CPU
35	/RD	In	/RD FROM CPU
36	/RFSH	In	/RFSH FROM CPU
37	/SMEMR	Out	VIDEO MEMORY READ (TO VGA CHIP)
38	/SMEMW	Out	VIDEO MEMORY WRITE (TO VGA CHIP)
39	GND		
40	/COE0		Not used
41	/IORD	Out	VGA IO READ (TO VGA CHIP)
42	/IOWR	Out	VGA IO WRITE (TO VGA CHIP)
43	/SBHE	Out	BUS HIGH ENABLE (TO VGA CHIP)
44	/VIO2	Out	VGA IO CHIP SELECT

3. Address map

3-1. Total memory space

The address map of the total memory space is shown below. The memory space is divided into the following blocks:

- 0page area (including the I/O area)
- VRAM
- RAM
- ROM
- Extended I/O area



The lower 64 KB or less of the Flash ROM area is mapped in the 0PAGE area. By mapping the ROM, it is possible to accommodate RESET and VECTOR ADDRESS.

∗ Internal and external I/Os of the CPU are, 8-bit and fixed to 3-states.

Used as VRAM area for LCDC.
VMEM2#: C80000H - 08FFFFH (128KB)
VIO2#: CE0000H - CFFFFFH

Expansion I/O area: Space for an I/O device which needs to be arranged in space other than the 0PAGE area.
MPCA8 uses the addresses from FFFF00H to FFFFFFH for an address specification register (BAR) for SSP.
The I/O register and printer buffer RAM and the TCP/IP dual port RAM are also located here.
VIO# (LCDC I/O): F10000H - F1FFFFH (Not used)
PBRAM: F00000H - F0FFFFH
DPCS# (TCP/IP): F20000H - F3FFFFH

Fig. 2

3-2. 0page area

The 0page area consists of three spaces: ① the ROM mapped area, ② internal and ③ external I/O areas.
The ROM mapped space have been devised for the following purposes:

① Simplifying the procedure for booting the IPL program

② Achieving high-speed accessing, and accessing by abbreviated instructions.

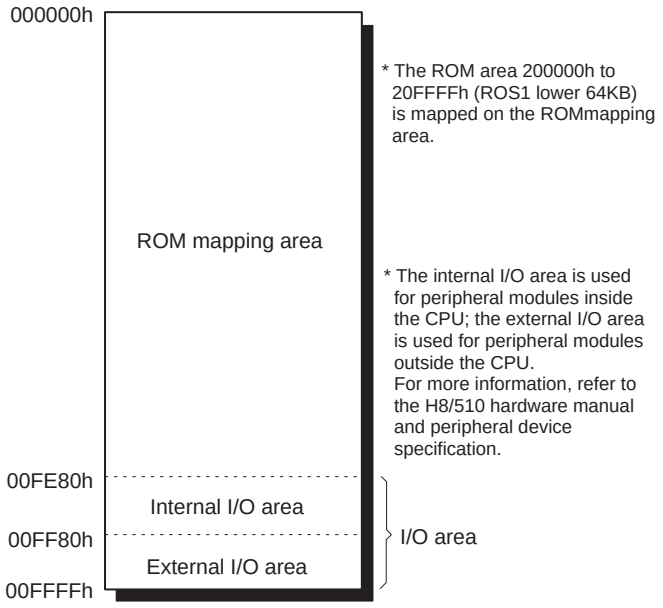

000000h
ROM mapping area
00FE80h
Internal I/O area
00FF80h
External I/O area
00FFFFh
I/O area
* The ROM area 200000h to 20FFFFh (ROS1 lower 64KB) is mapped on the ROMmapping area.
* The internal I/O area is used for peripheral modules inside the CPU; the external I/O area is used for peripheral modules outside the CPU.
For more information, refer to the H8/510 hardware manual and peripheral device specification.

Fig. 3

3-3. I/O areas

The addresses from 00FF80h to 00FFFFh are called the internal I/O area.
The internal I/O area is a space where the control registers and built-in ports inside the CPU are addressed.
The external I/O area is a space where the peripheral devices outside the CPU or devices on an optional card are addressed.

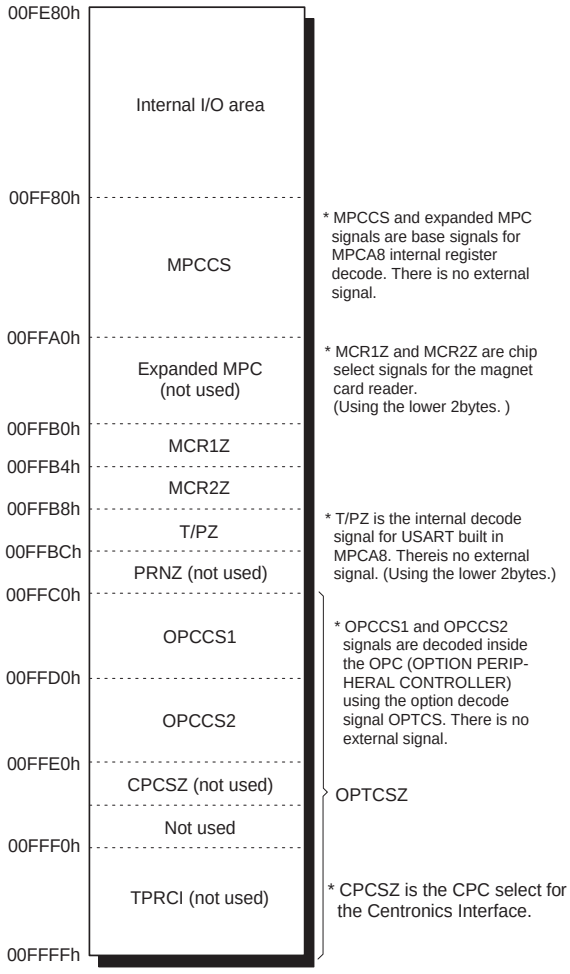

00FE80h
Internal I/O area
00FF80h
MPCCS
00FFA0h
Expanded MPC (not used)
00FFB0h
MCR1Z
00FFB4h
MCR2Z
00FFB8h
T/PZ
00FFBCh
PRNZ (not used)
00FFC0h
OPCCS1
00FFD0h
OPCCS2
00FFE0h
CPCSZ (not used)
Not used
00FFF0h
TPRCl (not used)
00FFFFh
OPTCSZ
* MPCCS and expanded MPC signals are base signals for MPCA8 internal register decode. There is no external signal.
* MCR1Z and MCR2Z are chip select signals for the magnet card reader.
(Using the lower 2bytes.)
* T/PZ is the internal decode signal for USART built in MPCA8. Thereis no external signal. (Using the lower 2bytes.)
* OPCCS1 and OPCCS2 signals are decoded inside the OPC (OPTION PERIP-HERAL CONTROLLER) using the option decode signal OPTCS. There is no external signal.
* CPCSZ is the CPC select for the Centronics Interface.

Fig. 4

3-4. ROM space

Fig.5 shows the ROM space. The UP-3301 uses 2MB of NOR-type flash memory instead of a conventional ROM, so that the ROS1 from the MPCA8 is input into the chip enable of the flash memory.

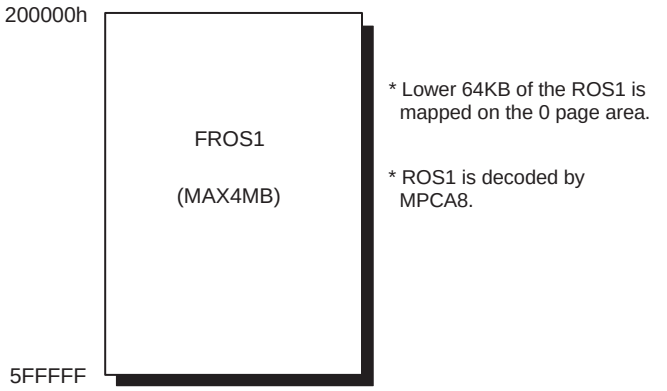


Fig. 5

3-5. VRAM & RAM space

The VRAM is the display memory of the LCD.

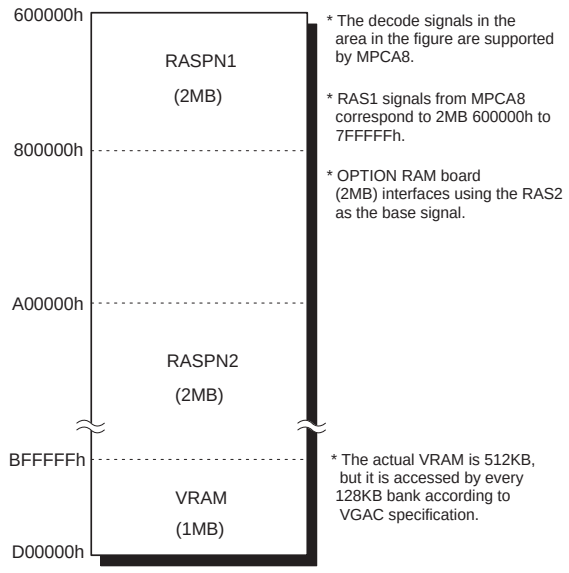

600000h
RASPN1
(2MB)
800000h
A00000h
RASPN2
(2MB)
BFFFFFh
VRAM
(1MB)
D00000h
* The decode signals in the area in the figure are supported by MPCA8.
* RAS1 signals from MPCA8 correspond to 2MB 600000h to 7FFFFFh.
* OPTION RAM board (2MB) interfaces using the RAS2 as the base signal.
* The actual VRAM is 512KB, but it is accessed by every 128KB bank according to VGAC specification.

Fig. 6

3-6. Extended I/O area

The addresses from F00000h to FFFFFFh are called an extended I/O area. The UP-3301 uses the following addresses as the break address register (BAR) for SSP.

- FFFF00h ~ FFFFFFh

4. LCD display

The main display is a 640 x 480 dot liquid crystal display.

4-1. Block diagram

Here is the block diagram of the LCD and its associated components.

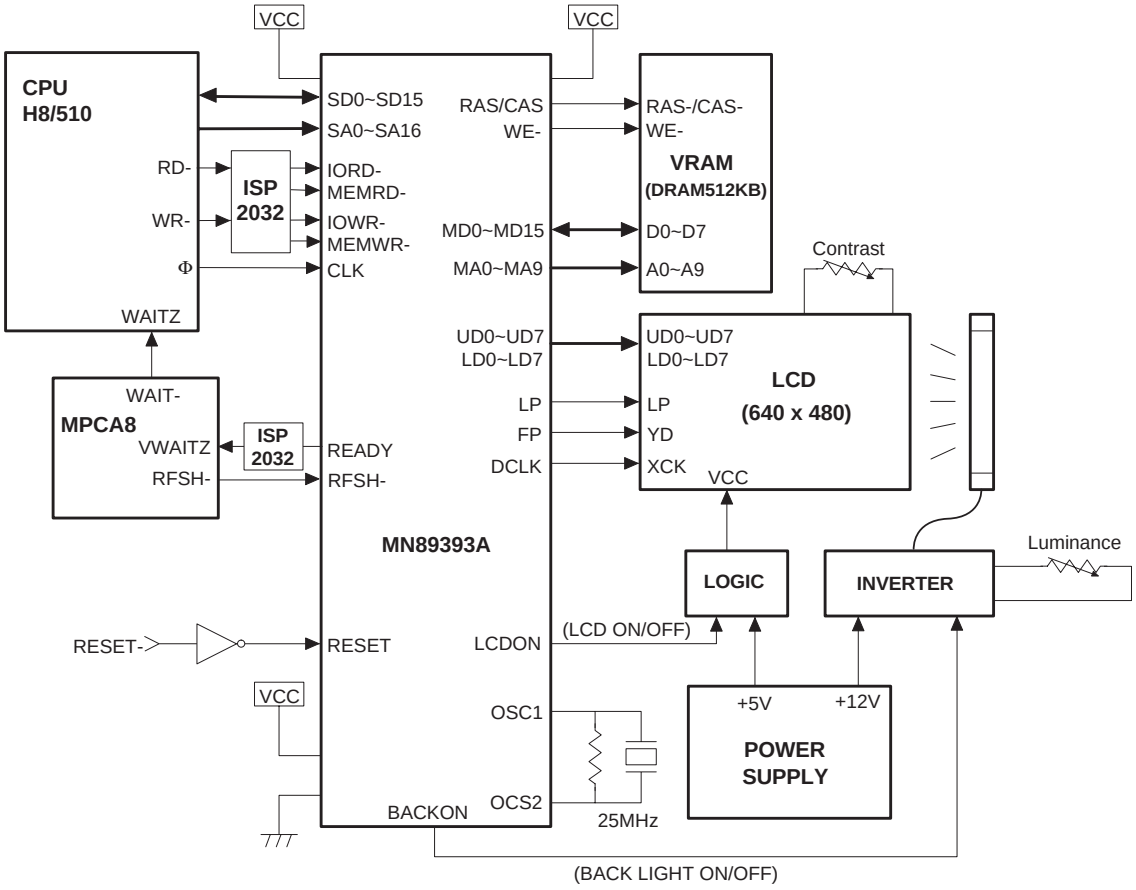


Fig. 7

4-2. LCD panel

The dot-matrix LCD unit LM10V33 with color STN and CCFT back light is used for the LCD panel. The resolution provided is 640 x 480.

4-3. Display controller

The Matsushita VGAC (MN89303A) is used for the display controller. VRAM is on the address space of the CPU and data can be written on and read from it by every 128 KB of bank at the address C00000H ~ C1FFFFH from the CPU side. VRAM consists of 4 banks.

4-4. LCD ON control

The LCD's bias power supply is controlled by the MN89303A terminal LCDON to turn the LCD screen on and off.
The LCDON is at "L" resetting +5V power is supplied to the LCD by setting the expanded function control register bit5 of MN89303A to "H" with software. The LCD screen isn't turned on until +5V is supplied.

4-5. Back light control

The back light is turned ON/OFF by the MN89303A. The initial value is "L" and the back light is off. By setting the expanded function control register bit6 of the MN89303A to "H", the inverter unit is turned on.

4-6. Luminance and contrast adjustment

- Luminance: Luminance is adjusted with an inverter which has a dimming function.
- Contrast: Contrast is adjusted by controlling the contrast adjustment voltage (VCON) of the LM10V33.

5. Customer display

The customer display uses the NEW TYPE 2 LINE vacuum fluorescent tube. The display is turned on and off by the CKDC9.

6. Pseudo SRAM (Standard)

The device is a TOSHIBA 4MB SRAM (TC51V8512AFT 512K x 8bit) with access time of 120ns.

6-1. CPU interface

The figure below shows a typical pseudo SRAM interface in the UP-3301.

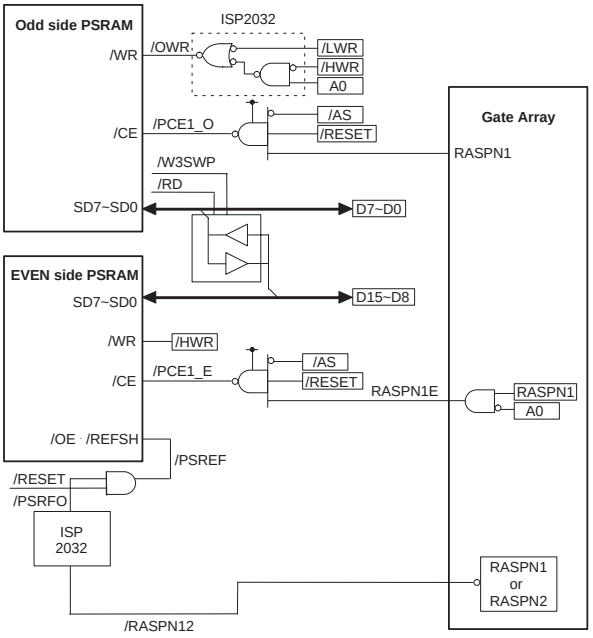


Fig. 8

6-2. Pseudo SRAM address

The standard pseudo SRAM is decoded as follows by the RASPN1 signal.

① 700000h ~ 7FFFFFh

The base signal is 2MB. Thus, it wraparounds with 600000H ~ 6FFFFFH 1MB.
The pseudo SRAM consists of 1 chip for respective even and odd number addresses. Both of word and byte access from CPU are available.

7. NOR-type flash memory

The NOR-type flash memory device is Sharp's LH28F016SU flash memory which consists of 512 K words x 16 or 1 MB x 8, with 16 blocks of 64 KB.

7-1. CPU interface

The figure below shows a typical interface for the LH28F016SU of the UP-3301 system.

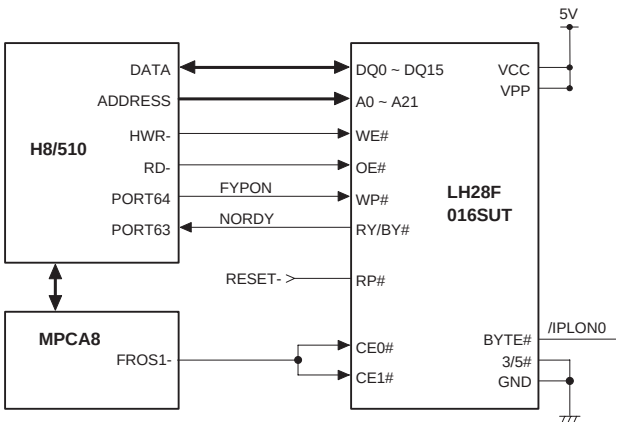


Fig. 9

7-2. Device control

After resetting, the device automatically enters the array read mode and perform the same action as the usual ROM, thus requiring no special consideration when reading data.
Data can be written at high speed by using the page buffer.

8. SSP control

The UP-3301 uses flash memory in the place of a EPROM, so it is possible to rewrite the contents of the flash memory when changing the program. However, since the existing MPCA8, it is also possible to use the conventional SSP.

8-1. Operation

Like the MPCA7, the MPCA8 adopts the break address register comparison method for detecting addresses. The operation of this method is briefly explained below.
The gate array always compares the break address register (BAR) built in the gate array, with the address bus to monitor the address bus.
If both agree, the gate array outputs the NMI signal to the CPU, which in turn shifts from normal handling to exception handling.
In both the MPCA7 and the MPCA8, SSP is achieved by the above operation.
The setting of the break address register (BAR) is directly written in the addresses from FFFF00h to FFFFFFh.

9. Interrupt control

There are roughly two types of interrupts:

- Internal interrupts: Controlled inside the CPU
- External interrupts: Input into the CPU from outside

9-1. Internal interrupts

Device interrupts built in the CPU are used for the following applications:

Table 8

Event factor		Application
SC11		Interrupt source as IR channel
SC12		Not used (SC1 is used for CKDC interface.)
FRT1	(ICI)	INTMCR ~ MCR interrupt (to FT11 terminal)
	(OCRA)	
	(OCRB)	
	(OVF)	
FRT2	(ICI)	Standard SHEN event (for CKDC)
	(OCRA)	Simple IRC timer event
	(OCRB)	RS232 timer event
	(OVF)	System timer (53 ms)
TMR	(CMA)	
	(CMB)	
	(OVF)	
WDT	(OVF)	Drawer open timer
A/D		Not used
NMI		SSP request

9-2. External interrupts

The following types of external interrupts are available:

- $\overline{\text{NMI}}$ (SSP)
- $\overline{\text{IRQ0}}$ (Standard I/O interrupt)
- $\overline{\text{IRQ1}}$ (RS232 interrupt)
- $\overline{\text{IRQ2}}$ (Used as SCK terminal)
- $\overline{\text{IRQ3}}$ (Used as SCK terminal)

10. WAIT control

The wait control function is built in the MPCA8 and is used to provide an interface with low-speed devices.

10-1. Block diagram

The block diagram of the wait control function is shown.

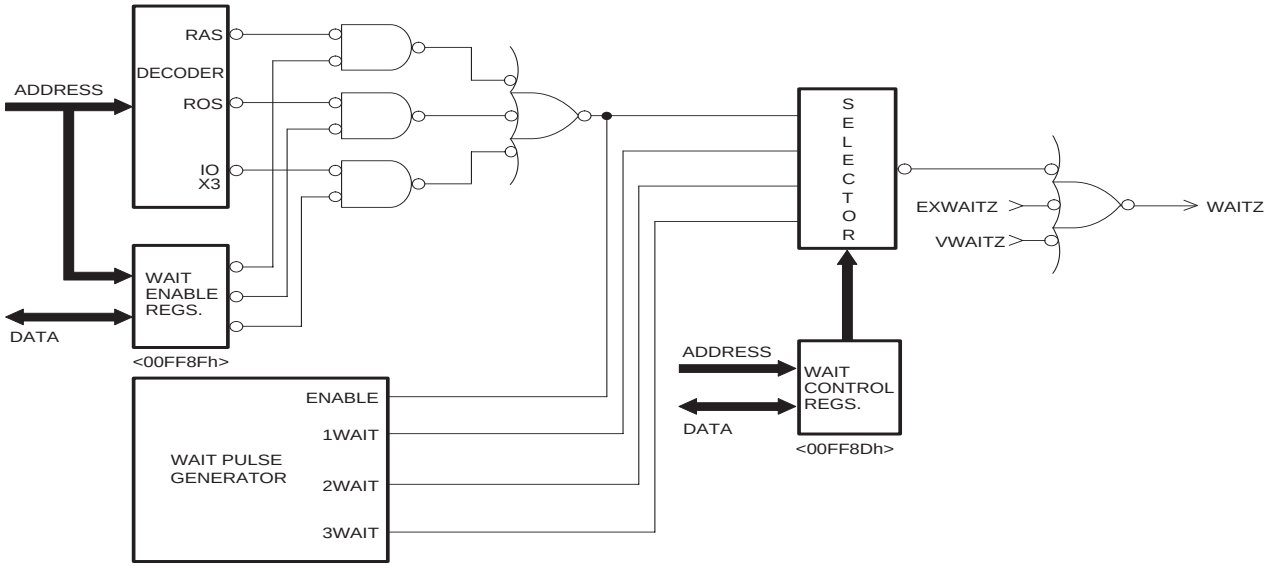


Fig. 10

In the figure, the decoder, wait enabling register, AND-OR sections are the same as those in the MPCA6 or 7, but other components are newly incorporated in the MPCA7.
EXWAITZ and WAITZ are external wait signals which are to be read inside the MPCA8 and output to the WAITZ. The EXWAITZ is a general-purpose wait request terminal, and WAITZ is the wait request signal from the VGA controller.

11. CKDC9

The UP-3301 performs the following controls, using the CKDC9.

- Customer display
- Clock
- Buzzer
- System reset

11-1. Interface

CKDC9 is connected through the MPCA8.

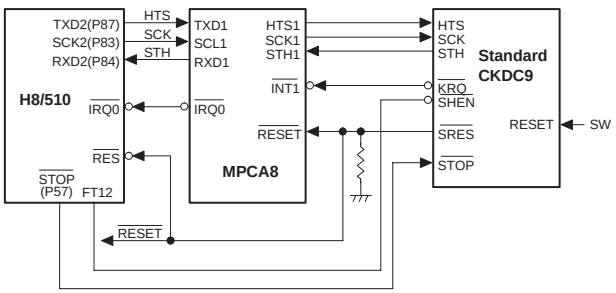


Fig. 11

12. Option RAM interface

12-1. Interface

The expanded RAM connector terminals are shown in the table.

The 72 pin S.O. DIMM is used for the connector.

Extension RAM connector terminals

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	1	–	25	D9	49
GND	2	–	26	D8	50
–	3	–	27	D7	51
–	4	–	28	D6	52
–	5	A13	29	D5	53
–	6	A12	30	D4	54
–	7	A11	31	D3	55
–	8	A10	32	D2	56
–	9	A9	33	D1	57
–	10	A8	34	D0	58
A14	11	A7	35	GND	59
A15	12	A6	36	NC	60
A16	13	A5	37	$\overline{OWR}$	61
A17	14	A4	38	–	62
A18	15	A3	39	–	63
A19	16	A2	40	–	64
–	17	A1	41	–	65
$\overline{PCE22\_E}$	18	A0	42	–	66
$\overline{PCE21\_E}$	19	D15	43	$\overline{HWR}$	67
–	20	D14	44	–	68
$\overline{RD}$	21	D13	45	VMEM	69
$\overline{PCE22\_O}$	22	D12	46	VMEM	70
$\overline{PCE21\_O}$	23	D11	47	GND	71
GND	24	D10	48	GND	72

13. Reset sequence

The reset sequence block diagram is shown below. Note that the $\overline{\text{RESET}}$ signal (system reset) and $\overline{\text{CKDCR}}$ signal (CKDC reset) are different from each other.

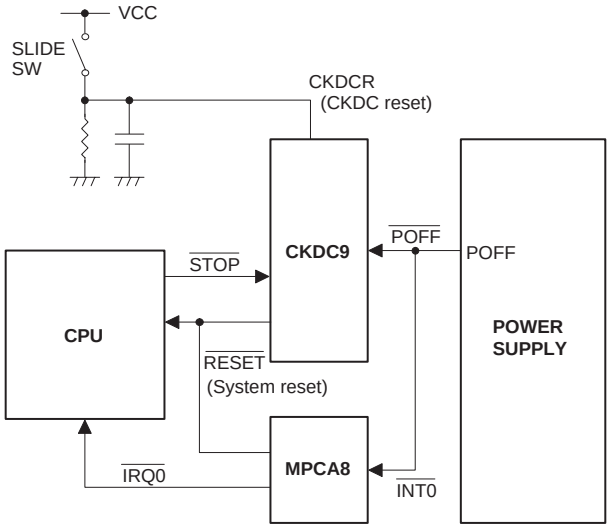


Fig. 14

13-1. Power ON/OFF

The flow of signal processing at the time of the power supply turning On/Off is as follows:

Table 19

<Power OFF>

	Power supply	MPCA8	CPU	CKDC9
1	$\overline{\text{POFF}}$ → L			
2		$\overline{\text{IRQ0}}$ → L		
3			$\overline{\text{STOP}}$ → L	
4				$\overline{\text{RESET}}$ → L (System reset)

Table 20

<Power ON>

	Power supply	MPCA8	CPU	CKDC9
1	$\overline{\text{POFF}}$ → H			
2				$\overline{\text{RESET}}$ → H (System reset)

The table below shows the timing chart.

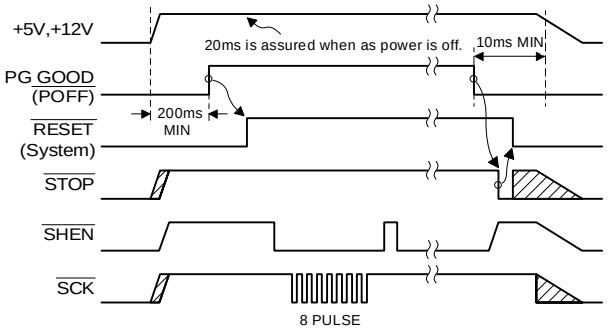


Fig. 15

13-2. MRS, SRV reset

In the UP-3301, the MRS, SRV resetting is selected and executed by the key which has been depressed when the CKDC reset is released to start the system.
(In the case of a MRS, security is added by a key operation equivalent to a password.)

Flow chart

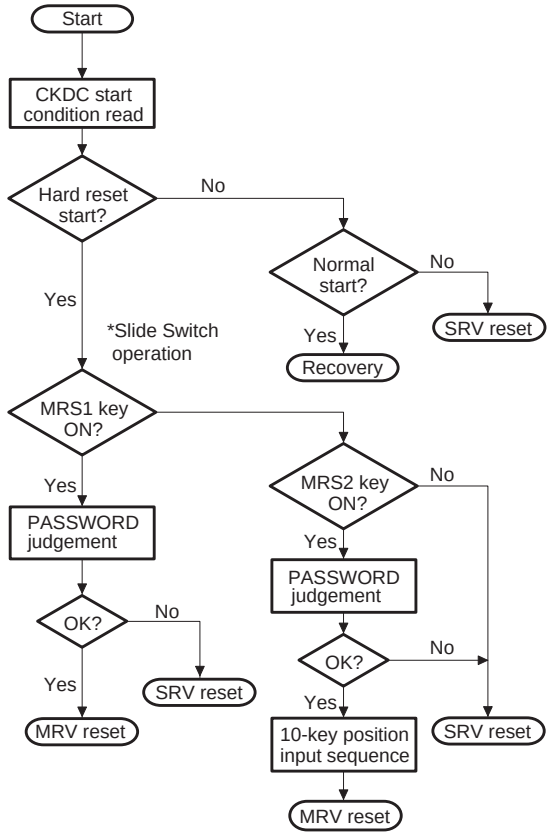


Fig. 16

14. Drawer

The UP-3301 can use up to 2 optional external drawers.

14-1. Drawer solenoid drive

P34 ~ P37 inside the CPU are allocated for the port output of the drawer solenoid drive.

Table 22

Built-in port	Signal name	Remarks
P34	$\overline{\text{DR0}}$	Drawer 1 (optional drawer)
P35	$\overline{\text{DR1}}$	Drawer 2 (optional drawer)
P36	$\overline{\text{DR2}}$	Reserved
P37	$\overline{\text{DR3}}$	Reserved

One port corresponds to one drawer. Theoretically, it is possible to drive multiple drawers at the same time, but this processing must be inhibited by using software, because of power supply capacity and driver hardware factors. If a power failure is detected, the drawer solenoid drive must be stopped as soon as possible.

∗The drawer solenoid drive time must be controlled in the range of 40 ms to 50 ms by the timer.

14-2. Drawer open/close sensor

The drawer open/close sensor signal is input into the built-in port of the CPU. The sensor signal of an optional drawer sensor is also wired read before inputting.

• P33=1: Any of the drawers is open.

15. RS232

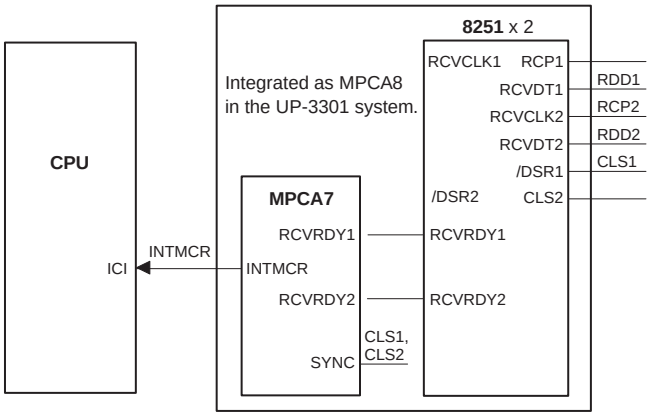
Two standard RS232 channels are compatible with the ER-A7RS2. However, while the ER-A7RS2 uses the $\overline{IRQ2}$ terminal of the CPU for interruption of the RS232, the UP-3301 cannot use the $\overline{IRQ1}$ terminal instead of it. (The $\overline{IRQ2}$ terminal is used for IR as the SCK1 terminal.)
The standard RS232 is fixed to the logic channels 1 and 2. To the built-in printer, logic channel 7 is assigned. Use the channels 3, 4, 5 and 6 for the ER-A7RS2.

16. MCR

This paragraph describes MCR option (UP-E12MR2) control defined by UP-3301 hardware architecture.
2 channels of the serial port (interchangeable with 8251) built in the MPCA8 are used. 2 tracks of data are read simultaneously. Supports is provided for the first and second tracks MCR of ISO. (UP-E12MR2)

16-1. CPU interface

The CPU interface for the USART (8251) and magnet card reader (MCM-21) in the UP-3301 system is shown below.



Signal description

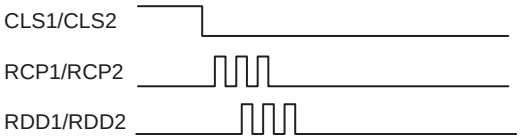
RCP1	TRACK 1 CLOCK PULSE
RDD1	TRACK 1 DATA SIGNAL
RCP2	TRACK 2 CLOCK PULSE
RDD2	TRACK 2 DATA SIGNAL
CLS1	TRACK 1 CARD DETECTION SIGNAL
CLS2	TRACK 2 CARD DETECTION SIGNAL
RCVRDY1	TRACK 1 DATA RECEIVING SIGNAL
RCVRDY2	TRACK 2 DATA RECEIVING SIGNAL
INTMCR	INTERRUPT SIGNAL OR-SYNTHESIZED from RCVRDY and SYNC input

2 chip select signals for the 8251 are generated inside the MPCA8. The 8251 write recovery time is as follows:

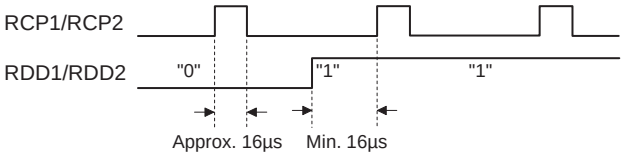
16-2. MCR interface

The operating timing of the MCR interface signals is given below.

(1) Example of timing



(2) Detailed timing (relation between DATA and CLOCK PULSE)



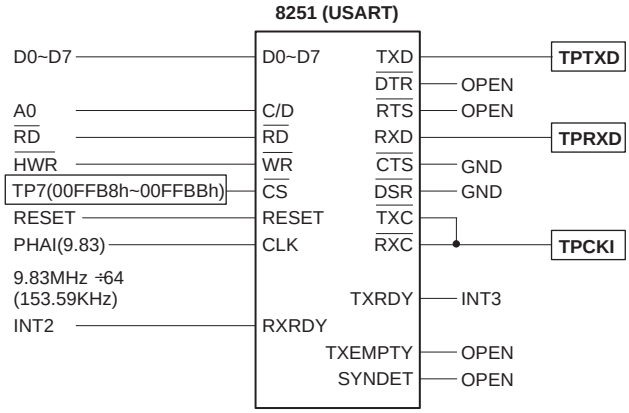
The “NULL” CODE is written prior to the opening code. The opening code detection algorithm is considered because data may become corrupt before and after the CARD detection signal due to a worn magnet stripe.

17. Touch panel interface

The 8251 built in the MPCA8 is used in serial communications with the touch panel controller.

8251 (TPZ): Located in 00FFB8h ~ 00FFBBh.

Interrupt: Signal sending interrupt is connected to the INT3.
Signal receiving interrupt is connected to the INT2.



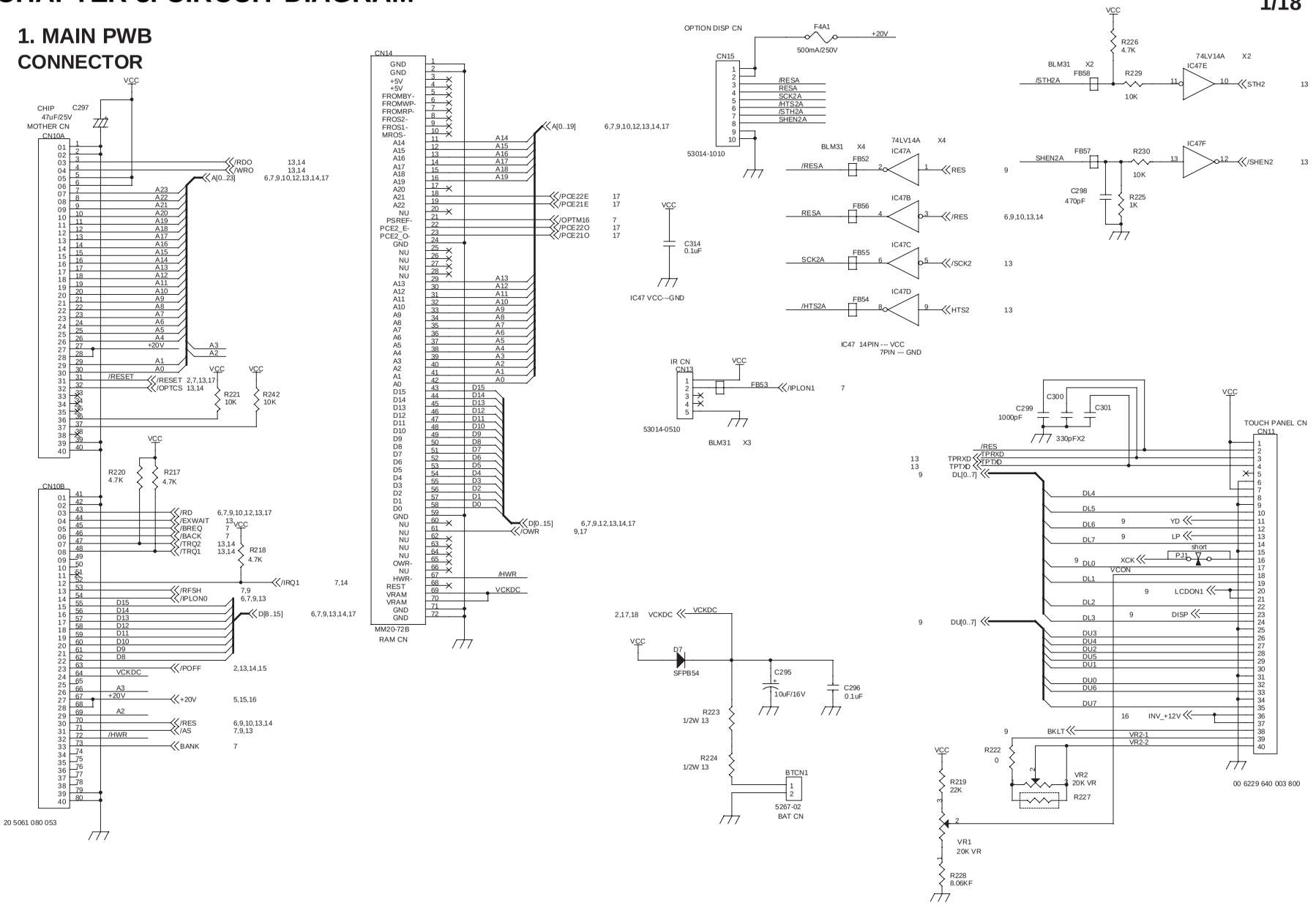
① Duplex type: Full-duplex
② Data rate: 9600 Bps
③ Synchronizing mode: Asynchronous
④ Signal level: TTL
⑤ Data format: 1 Start-bit
8 Data-bit
Stop-bit
Non parity-bit

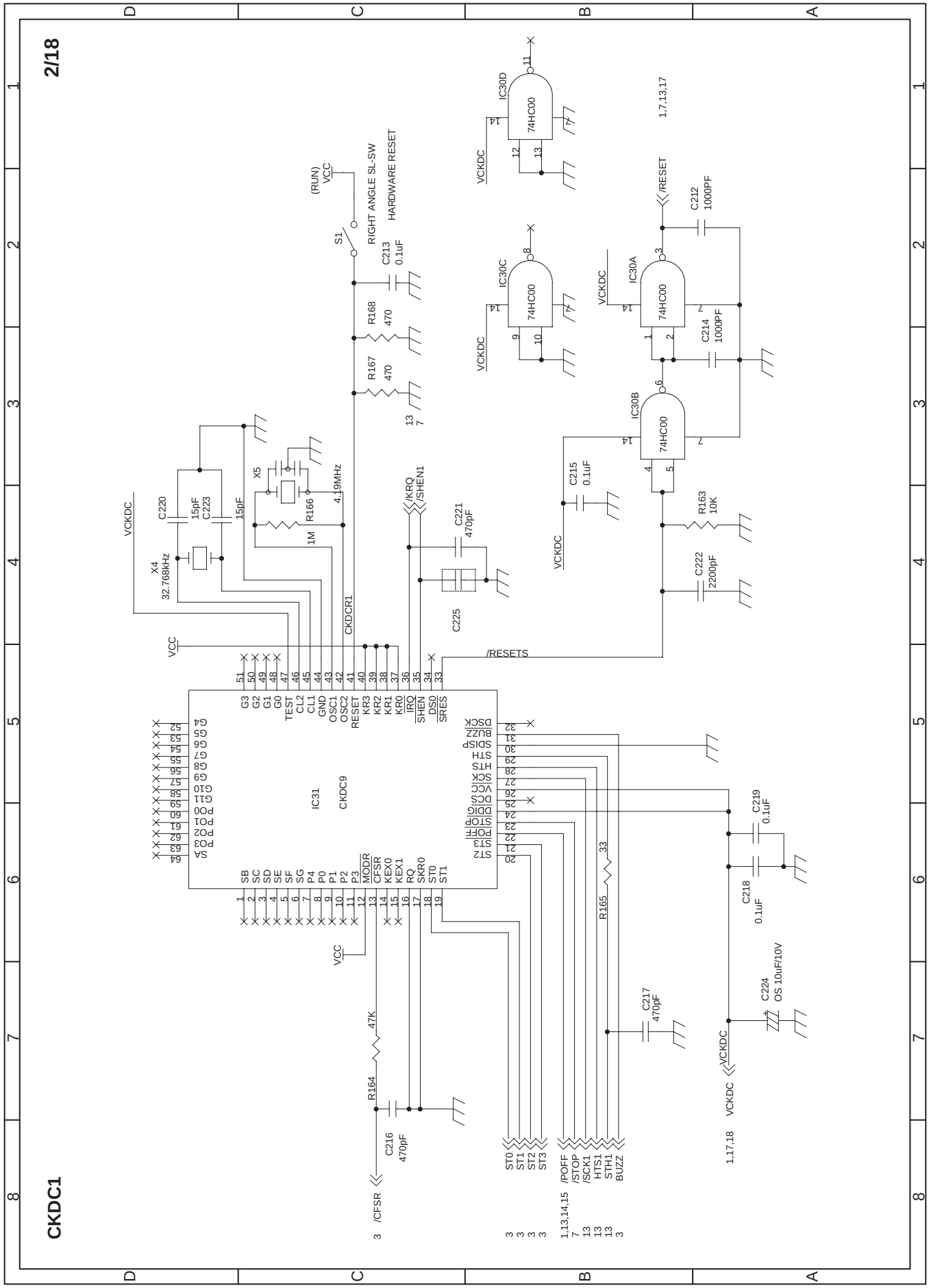
CHAPTER 8. CIRCUIT DIAGRAM

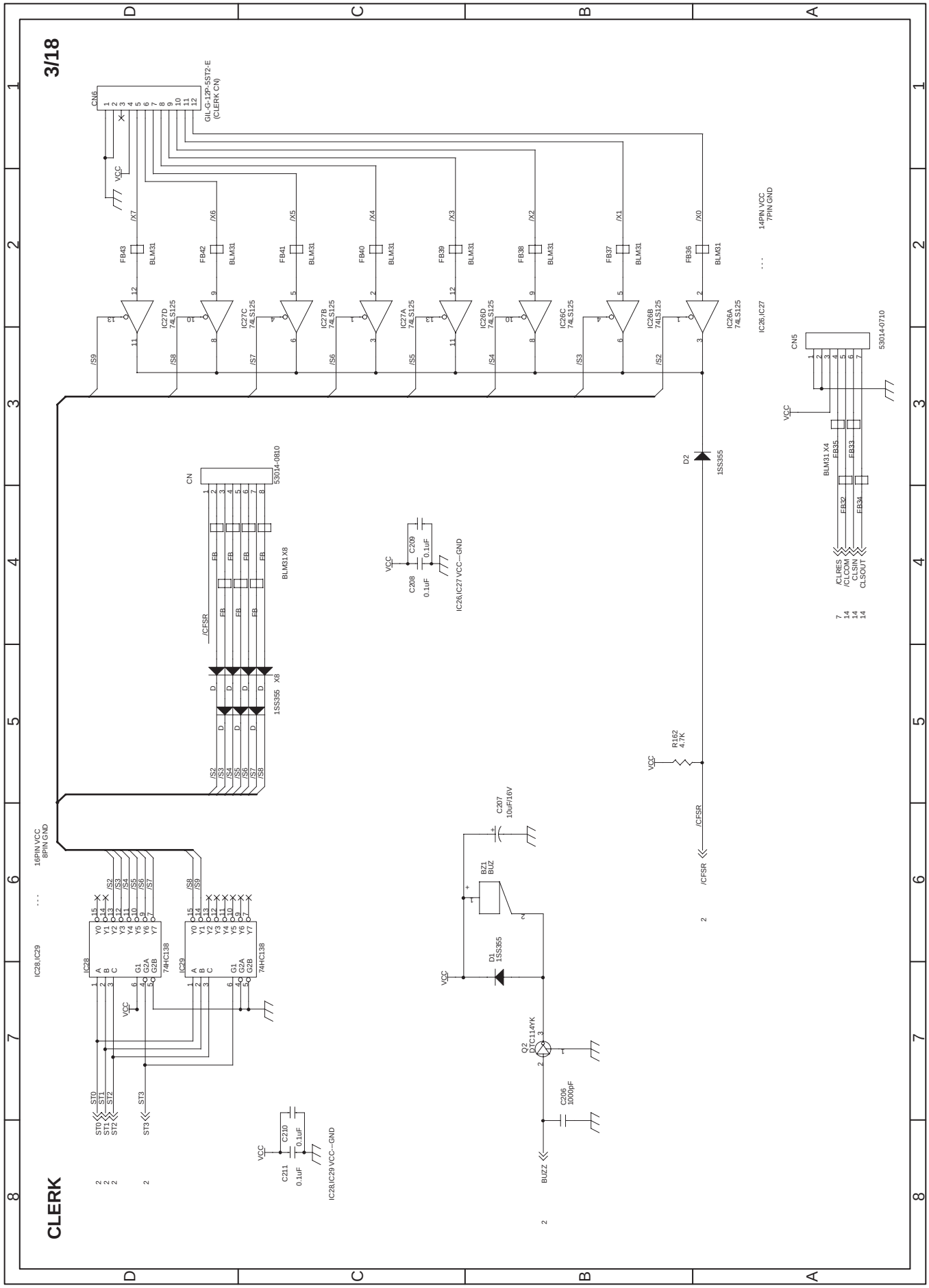
1/18

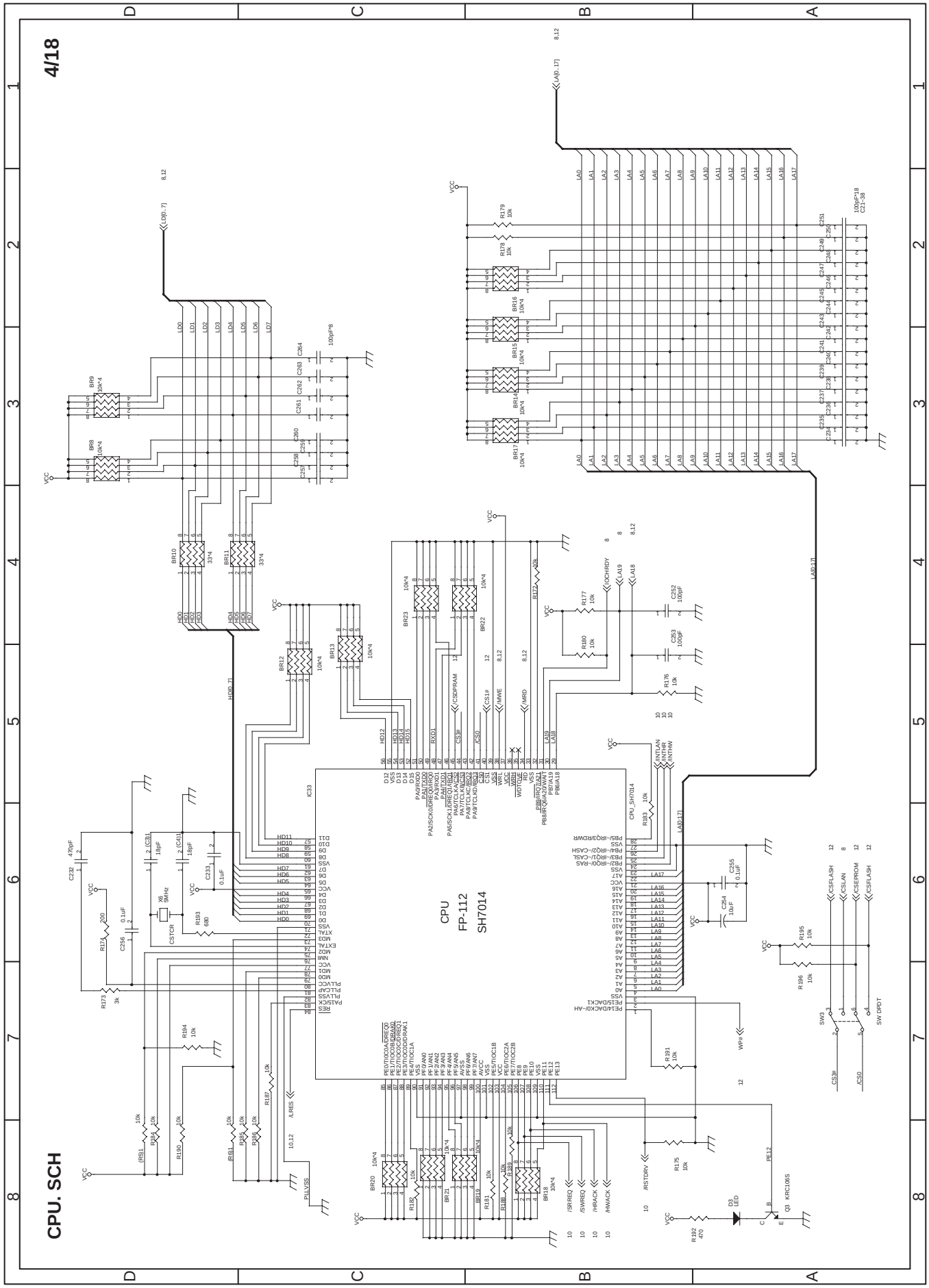
1. MAIN PWB

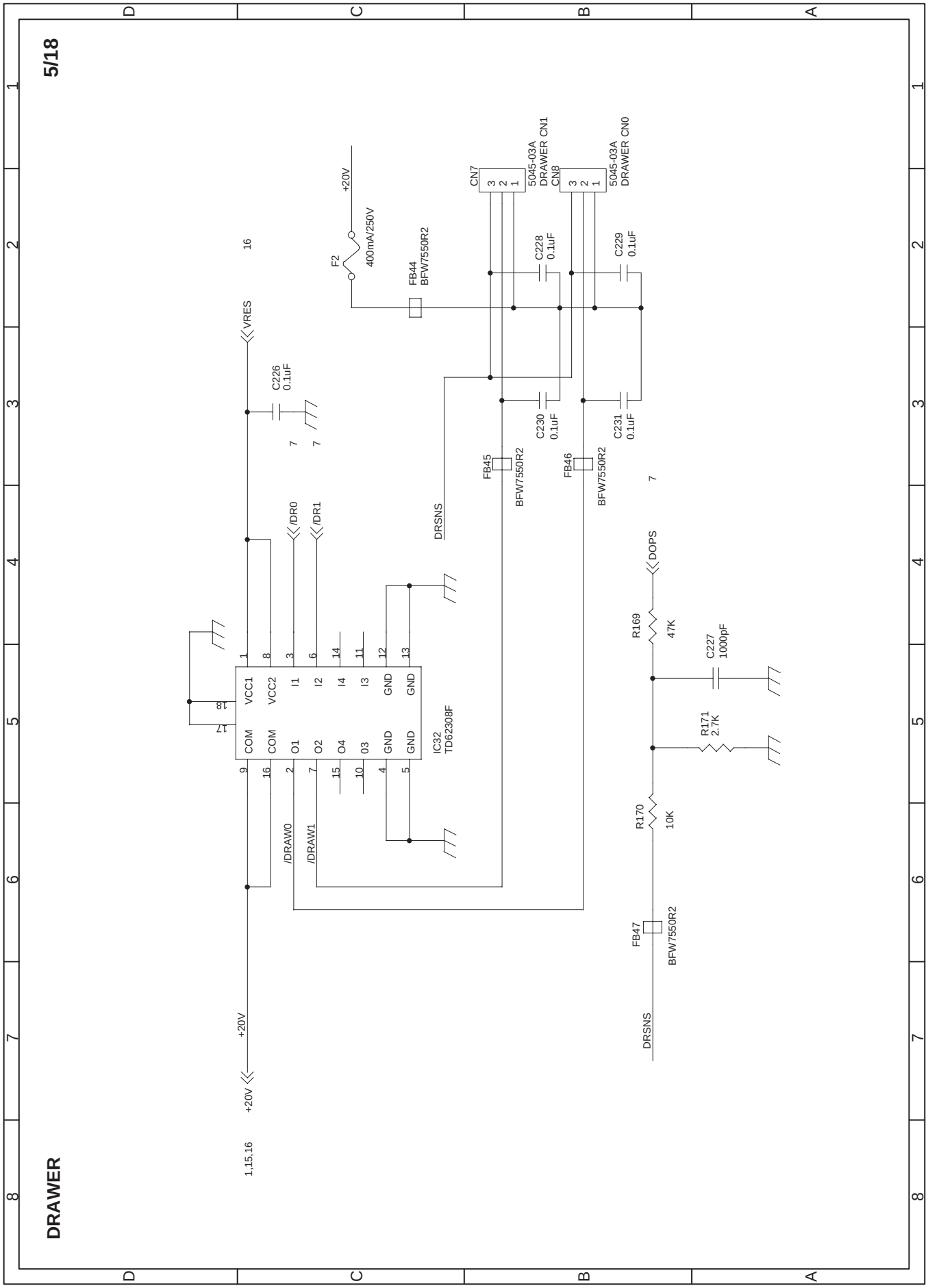
CONNECTOR

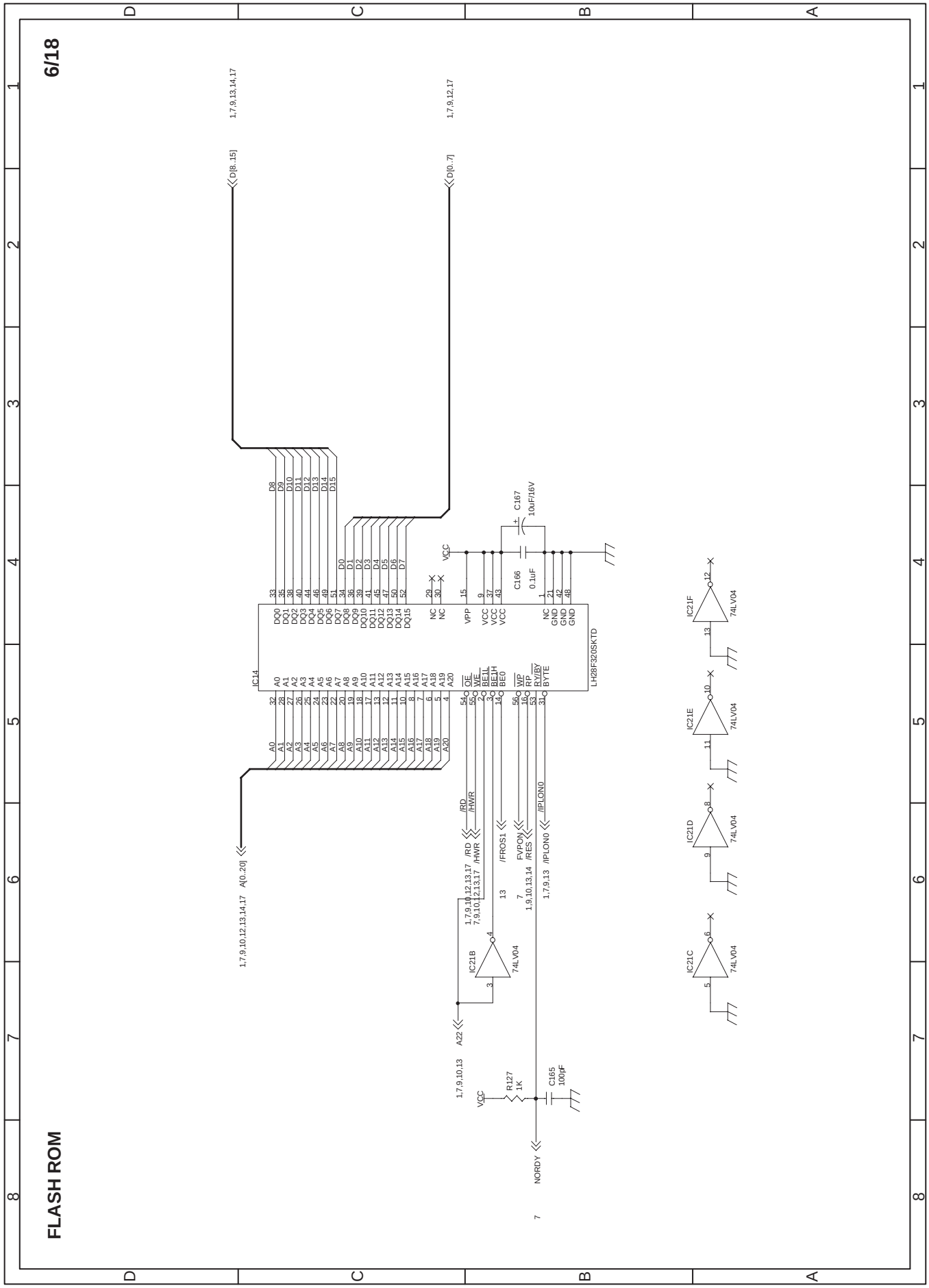


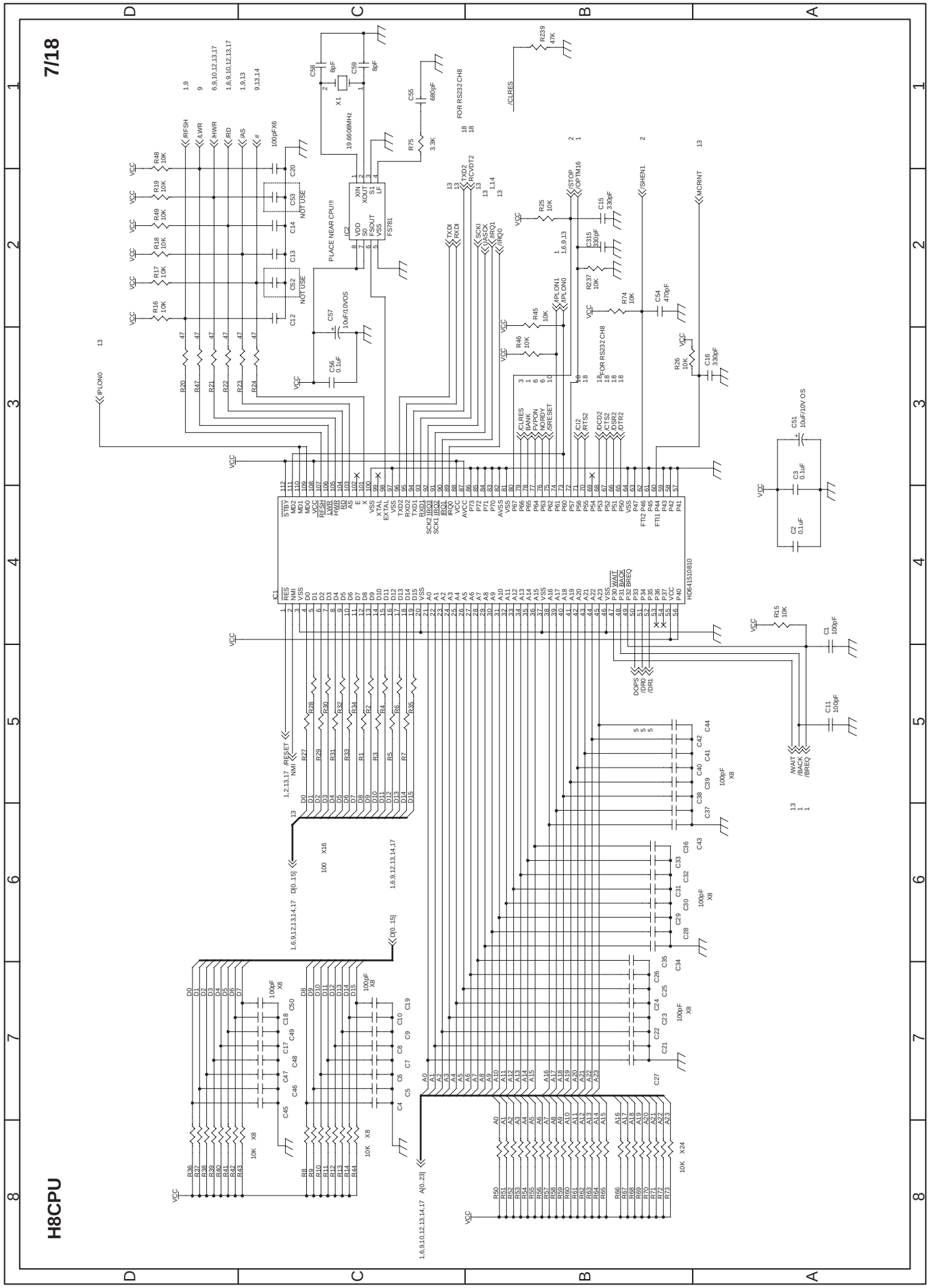

CKDC1
2/18
IC31
CKDC9
74HC00
IC30A
IC30B
IC30C
IC30D
X4
32.768kHz
X5
4.19MHz
S1
RIGHT ANGLE SL-SW
HARDWARE RESET
(RUN)
VCC
VCKDC
/RESET
/RESETS
/KRQ
/SHEN1
CKDCR1
/CFSR
/POFF
/STOP
/SCK1
HTS1
STH1
BUZZ
VCKDC
1.17,18
1.7,13,17
R163 10K
R164 47K
R165 33
R166 1M
R167 470
R168 470
C212 1000PF
C213 0.1uF
C214 1000PF
C215 0.1uF
C216 470pF
C217 470pF
C218 0.1uF
C219 0.1uF
C220 15pF
C221 470pF
C222 2200pF
C223 15pF
C224 OS 10uF/10V
C225

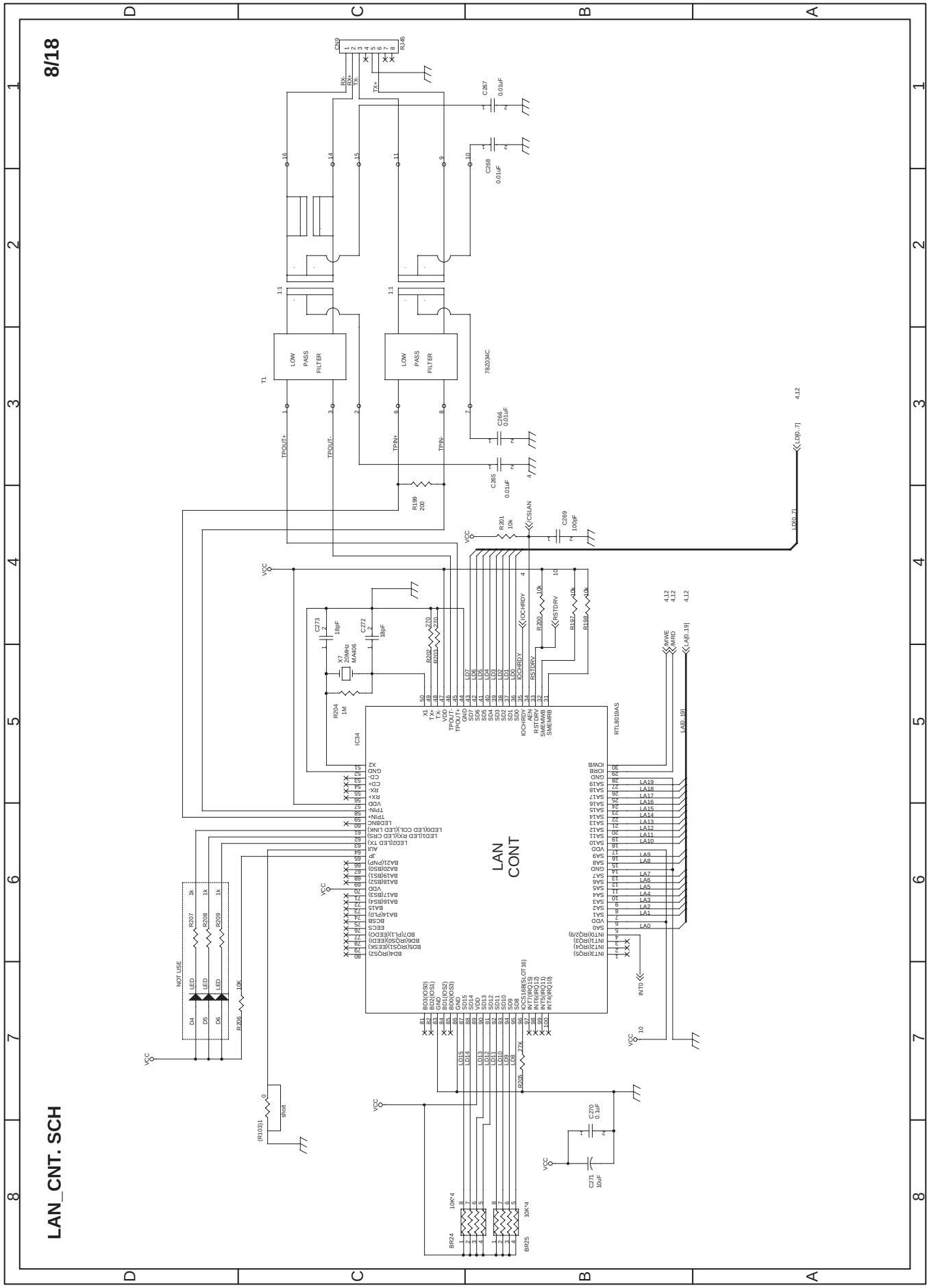

3/18
CLERK
CN6
GIL-G-12P-5ST2-E
(CLERK CN)
VCC
/X7
/X6
/X5
/X4
/X3
/X2
/X1
/X0
FB43
FB42
FB41
FB40
FB39
FB38
FB37
FB36
BLM31
IC27D 74LS125
IC27C 74LS125
IC27B 74LS125
IC27A 74LS125
IC26D 74LS125
IC26C 74LS125
IC26B 74LS125
IC26A 74LS125
IC26,IC27
14PIN VCC
7PIN GND
/S9
/S8
/S7
/S6
/S5
/S4
/S3
/S2
CN5
53014-0710
BLM31 X4
FB35
FB33
FB32
FB34
/CLRES
/CLCOM
CLSIN
CLSOUT
D2
1SS355
CN
53014-0810
BLM31 X8
/CFSR
1SS355 X8
C208
0.1uF
C209
0.1uF
IC26,IC27 VCC--GND
R162
4.7K
C207
10uF/16V
BZ1
BUZ
D1
1SS355
Q2
DTC114YK
C206
1000pF
BUZ2
16PIN VCC
8PIN GND
IC28,IC29
IC28
IC29
74HC138
ST0
ST1
ST2
ST3
C210
0.1uF
C211
0.1uF
IC28,IC29 VCC--GND

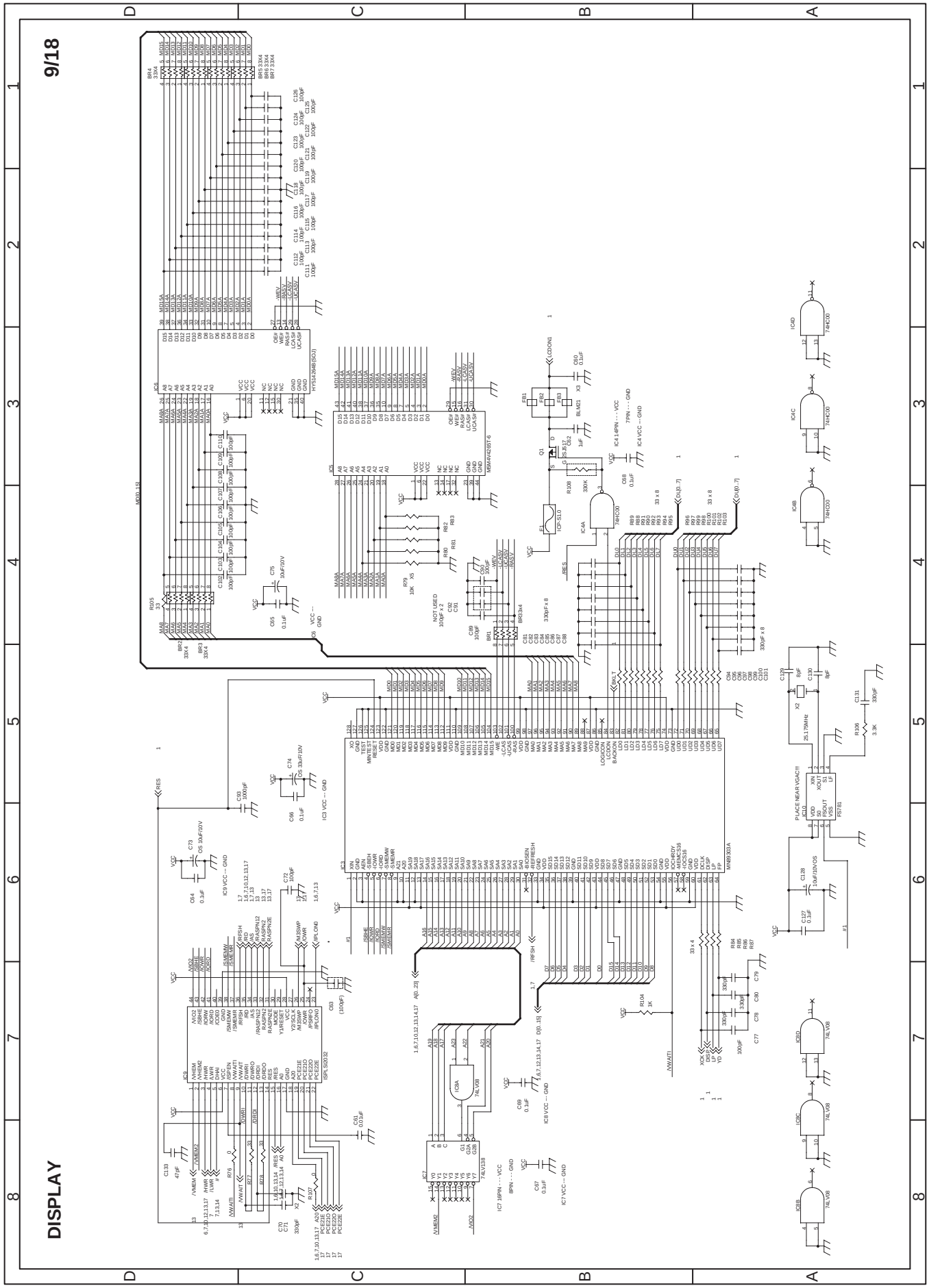

CPU. SCH
4/18
CPU
FP-112
SH7014
IC33
CPU_SH7014
VCC
GND
HD[0..7]
HD[0..15]
LA[0..17]
LD[0..7]
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
HD8
HD9
HD10
HD11
HD12
HD13
HD14
HD15
LA0
LA1
LA2
LA3
LA4
LA5
LA6
LA7
LA8
LA9
LA10
LA11
LA12
LA13
LA14
LA15
LA16
LA17
LA18
LA19
BR8
BR9
BR10
BR11
BR12
BR13
BR14
BR15
BR16
BR17
BR18
BR19
BR20
BR21
BR22
BR23
10k*4
33*4
X6
5MHz
C57CR
C232
C233
C234
C235
C236
C237
C238
C239
C240
C241
C242
C243
C244
C245
C246
C247
C248
C249
C250
C251
C252
C253
C254
C255
C256
C259
C260
C261
C262
C263
C264
C298
C299
100pF*8
100pF*18
C21-38
0.1uF
10uF
100pF
470pF
18pF
R173
R174
R175
R176
R177
R178
R179
R180
R181
R182
R183
R184
R185
R186
R187
R188
R189
R190
R191
R192
R193
R194
R195
R196
3k
200
680
470
10k
SW3
SW DPDT
D3
LED
Q8
KRC106S
/CSFLASH
/CSLAN
/CSEEPROM
/CSFLASH
/CS3P
/CS0
/CS1P
/CS3PRAM
/MWE
/MRD
/OCHRDY
/INTLAN
/INTHR
/INTHW
/RSTDRV
/SIRREQ
/SWREQ
/HRACK
/HWACK
ALRES
PLLVSS
WP#
UP-3301VS CIRCUIT DIAGRAM
– 67 –


5/18
DRAWER
+20V
400mA/250V
F2
FB44
BFW7550R2
CN7
5045-03A
DRAWER CN1
CN8
5045-03A
DRAWER CN0
C228
0.1uF
C229
0.1uF
C230
0.1uF
C231
0.1uF
FB45
BFW7550R2
FB46
BFW7550R2
DRSNS
VRES
C226
0.1uF
/DR0
/DR1
IC32
TD62308F
VCC1
VCC2
COM
COM
I1
I2
I4
I3
GND
GND
O1
O2
O4
03
/DRAW0
/DRAW1
DOPS
R169
47K
C227
1000pF
R171
2.7K
R170
10K
FB47
BFW7550R2
DRSNS
+20V
+20V
1,15,16


6/18
FLASH ROM
D[8..15]
D[0..7]
A[0..20]
IC14
LH28F320SKTD
C167
10uF/16V
C166
0.1uF
VCC
NC
NC
VPP
VCC
VCC
VCC
NC
GND
GND
GND
/RD
/HWR
/FROS1
FVPON
/RES
/IPLON0
BYTE
A22
IC21B
74LV04
R127
1K
C165
100pF
NORDY
IC21C
IC21D
IC21E
IC21F

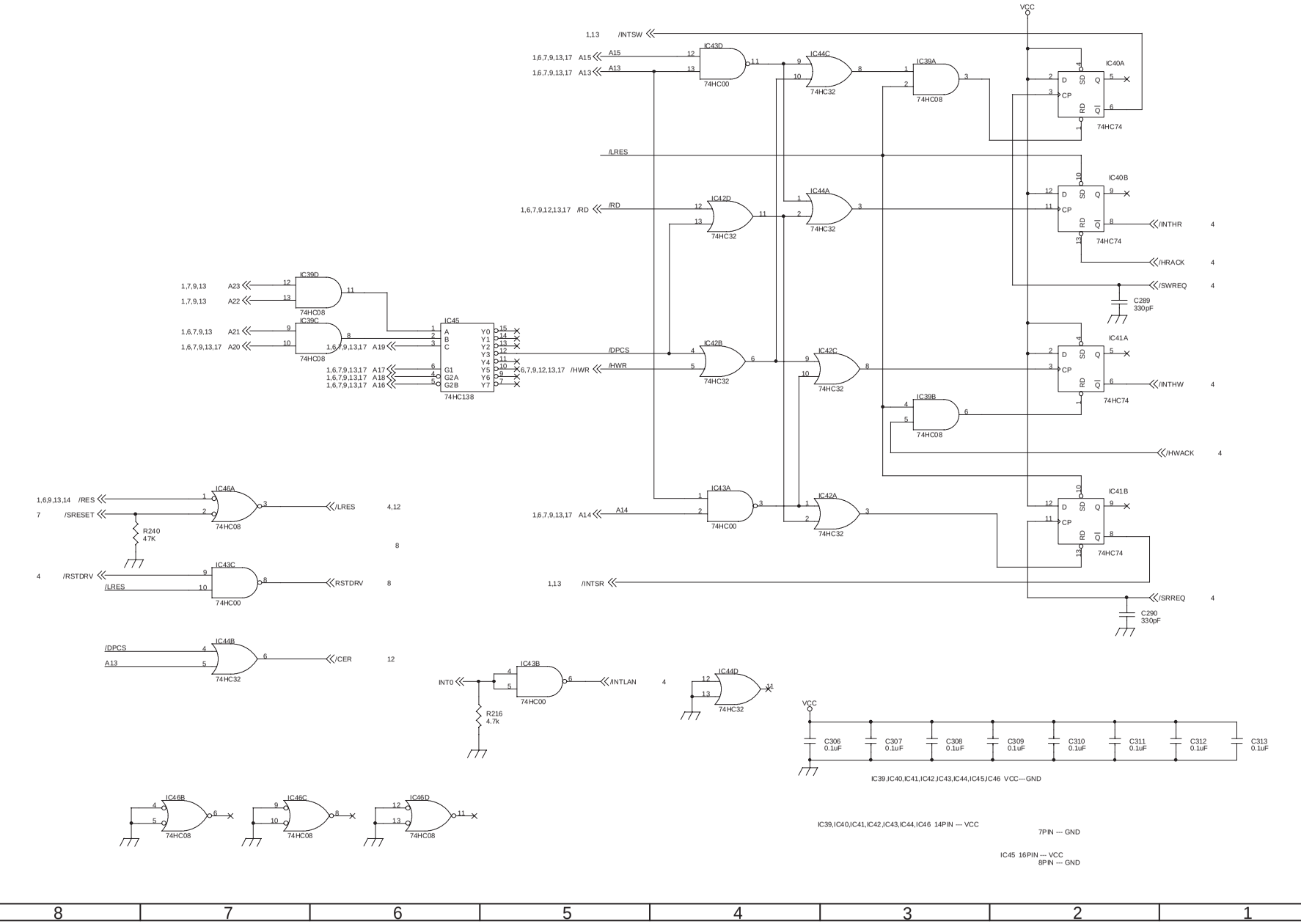

H8CPU
7/18
HD64151O810
X1
19.6608MHz
FS78L
PLACE NEAR CPU!!!
FOR RS232 CH8
NOT USE
/CLRES
/STOP
/OPTM16
/SHEN1
/MCRINT
/IPLON0
/IPLON1
/IPLON2
/RESET
/RFSH
/LWR
/HWR
/RD
/AS
/WAIT
/BACK
/BREQ
DOPS
/DR0
/DR1
VCC

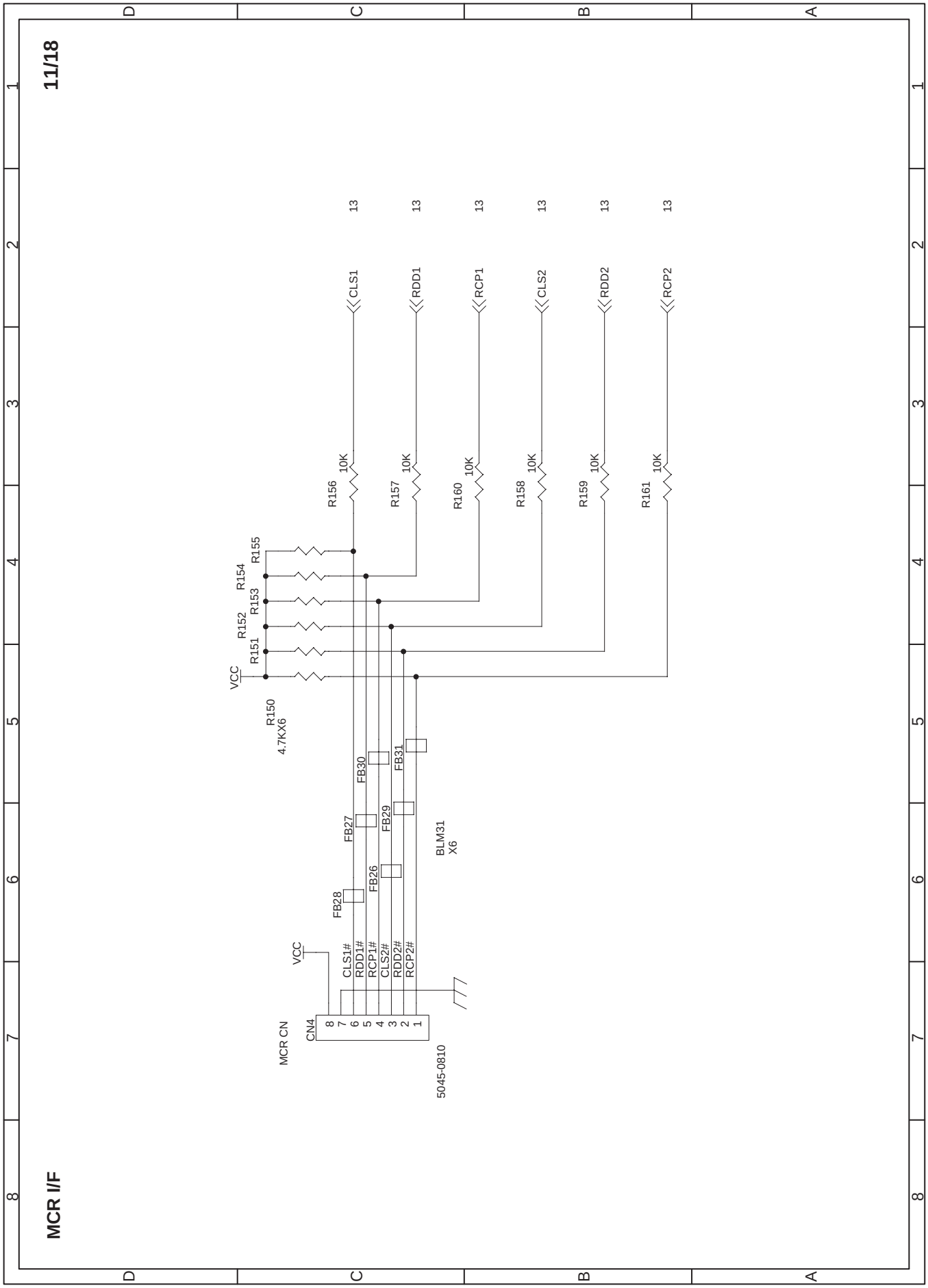

8/18
LAN_CNT. SCH
LAN
CONT
RTL8019AS
IC34
T1
LOW
PASS
FILTER
78Z034C
RJ45
TPOUT+
TPOUT-
TPIN+
TPIN-
/CSLAN
VCC
LD[0..7]
LA[0..19]
/MWE
/MRD
/IOCHRDY
RSTDRV
NOT USE
LED
D4
D5
D6
R207
R208
R209
R206
10K
1k
BR24
BR25
10K*4
X7
20MHz
MA406
C270
0.1uF
C271
10uF
C269
100pF
R201
10k
R199
200
C265
C266
C267
C268
0.01uF
R204
1M
R202
R203
270
C272
C273
18pF
R197
R198
R200
INT0
INT1(IRQ3)
INT2(IRQ4)
INT3(IRQ5)
INT4(IRQ10)
INT5(IRQ11)
INT6(IRQ12)
INT7(IRQ15)
4.12
10

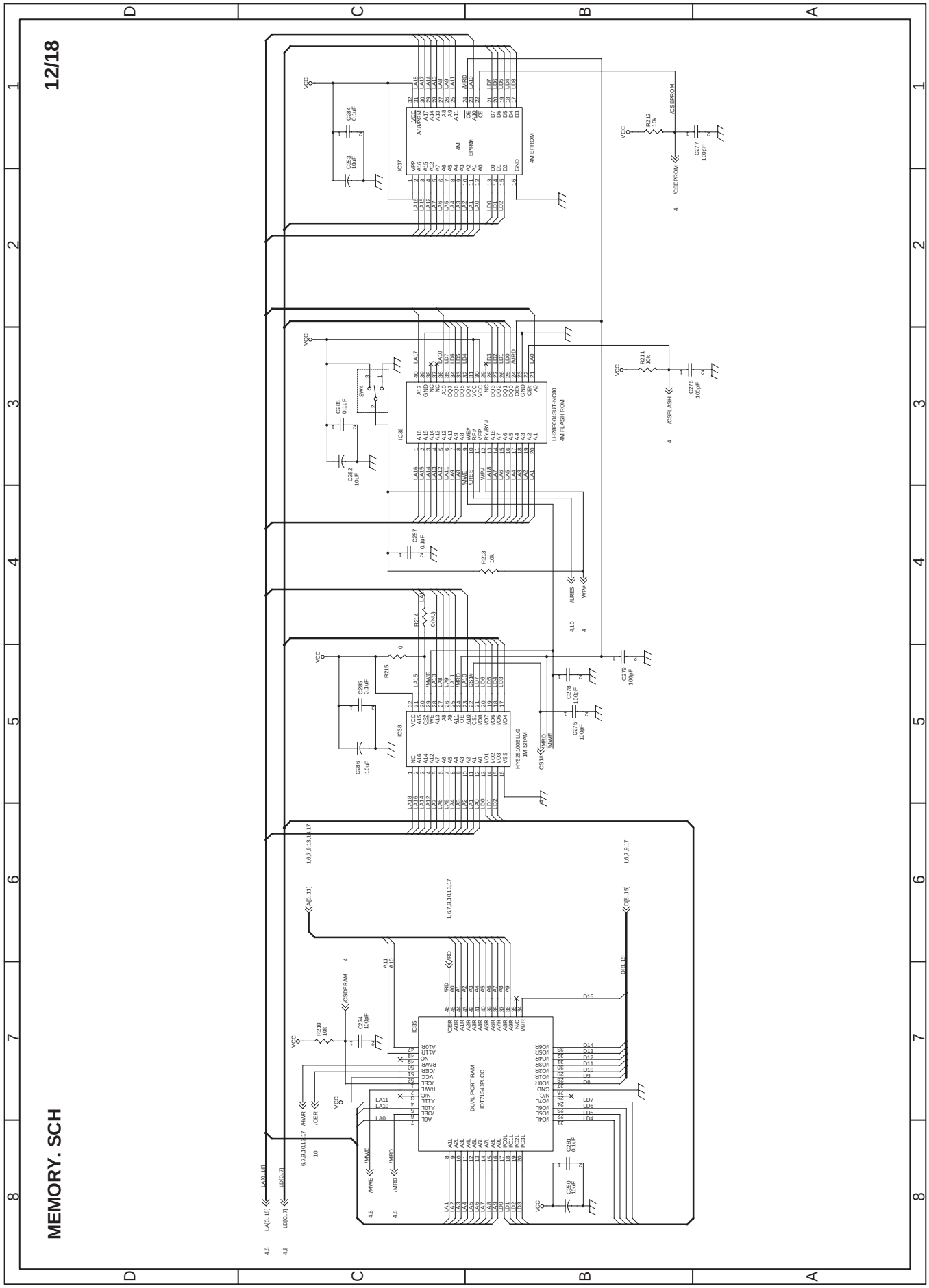

DISPLAY
9/18

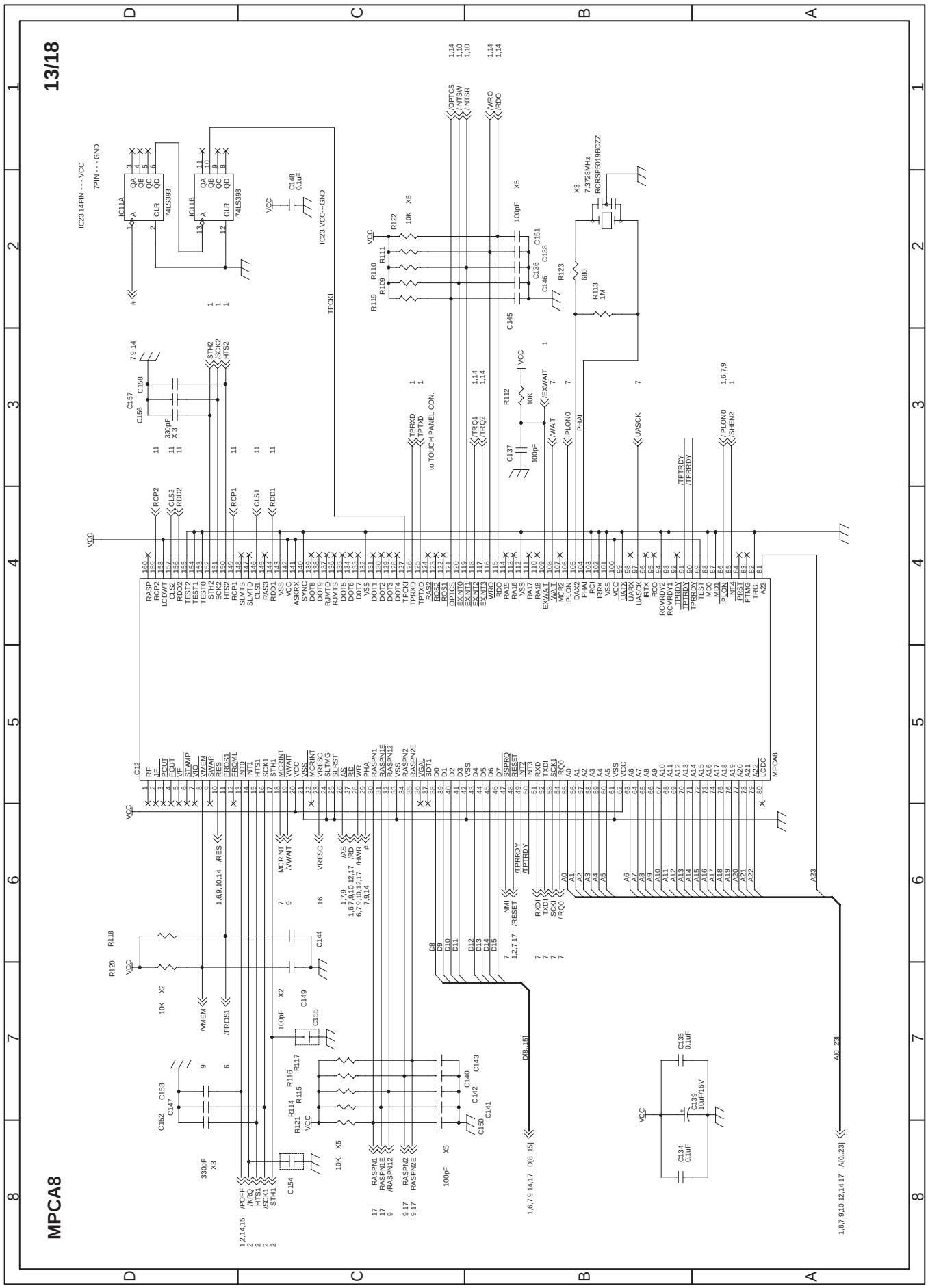
ISA_FPGA. SCH

10/18



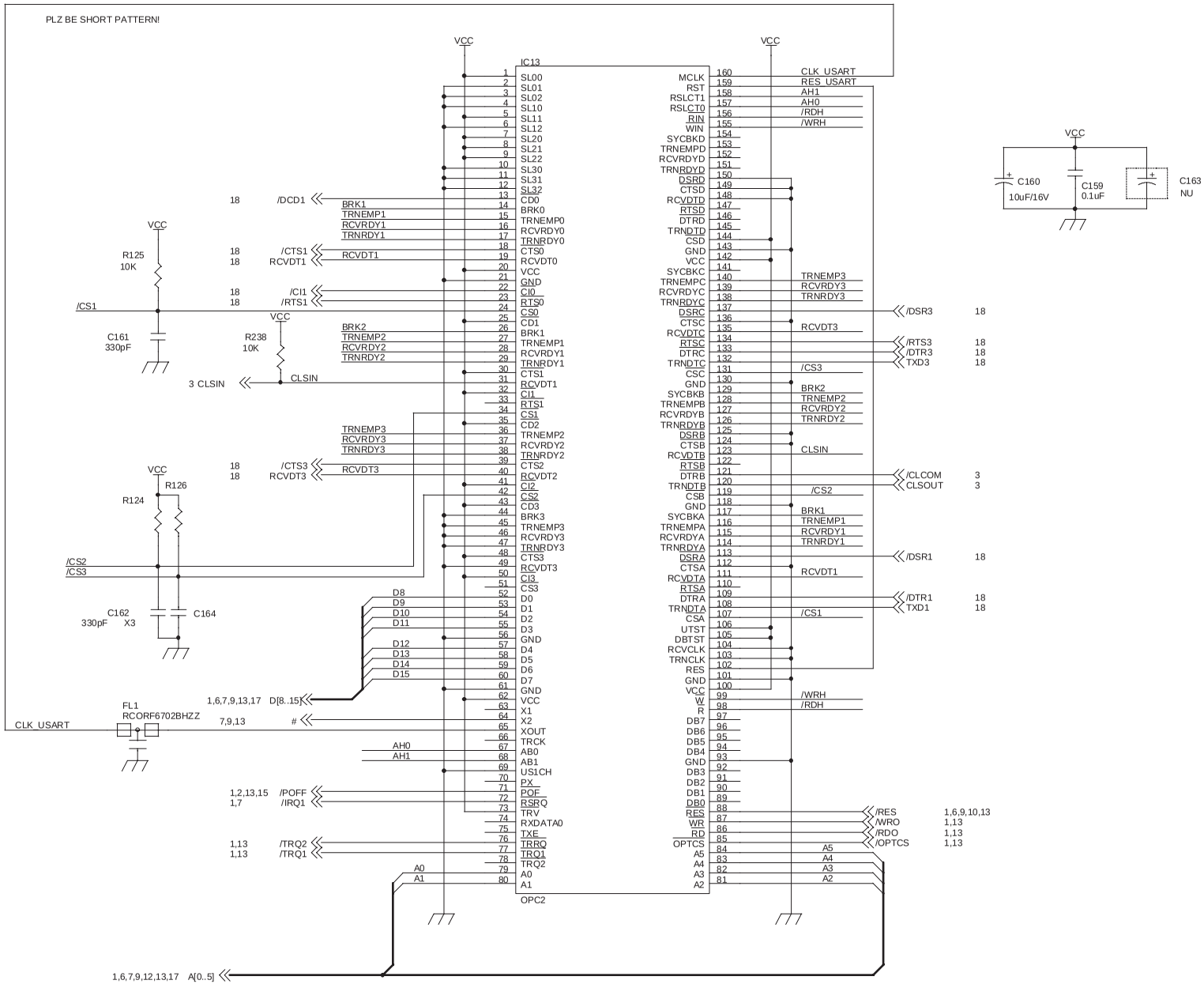

11/18
MCR I/F
CLS1
RDD1
RCP1
CLS2
RDD2
RCP2
13
R156
R157
R160
R158
R159
R161
10K
R155
R154
R153
R152
R151
VCC
R150
4.7KX6
FB30
FB31
FB27
FB29
FB26
FB28
BLM31
X6
CLS1#
RDD1#
RCP1#
CLS2#
RDD2#
RCP2#
MCR CN
CN4
8
7
6
5
4
3
2
1
5045-0810

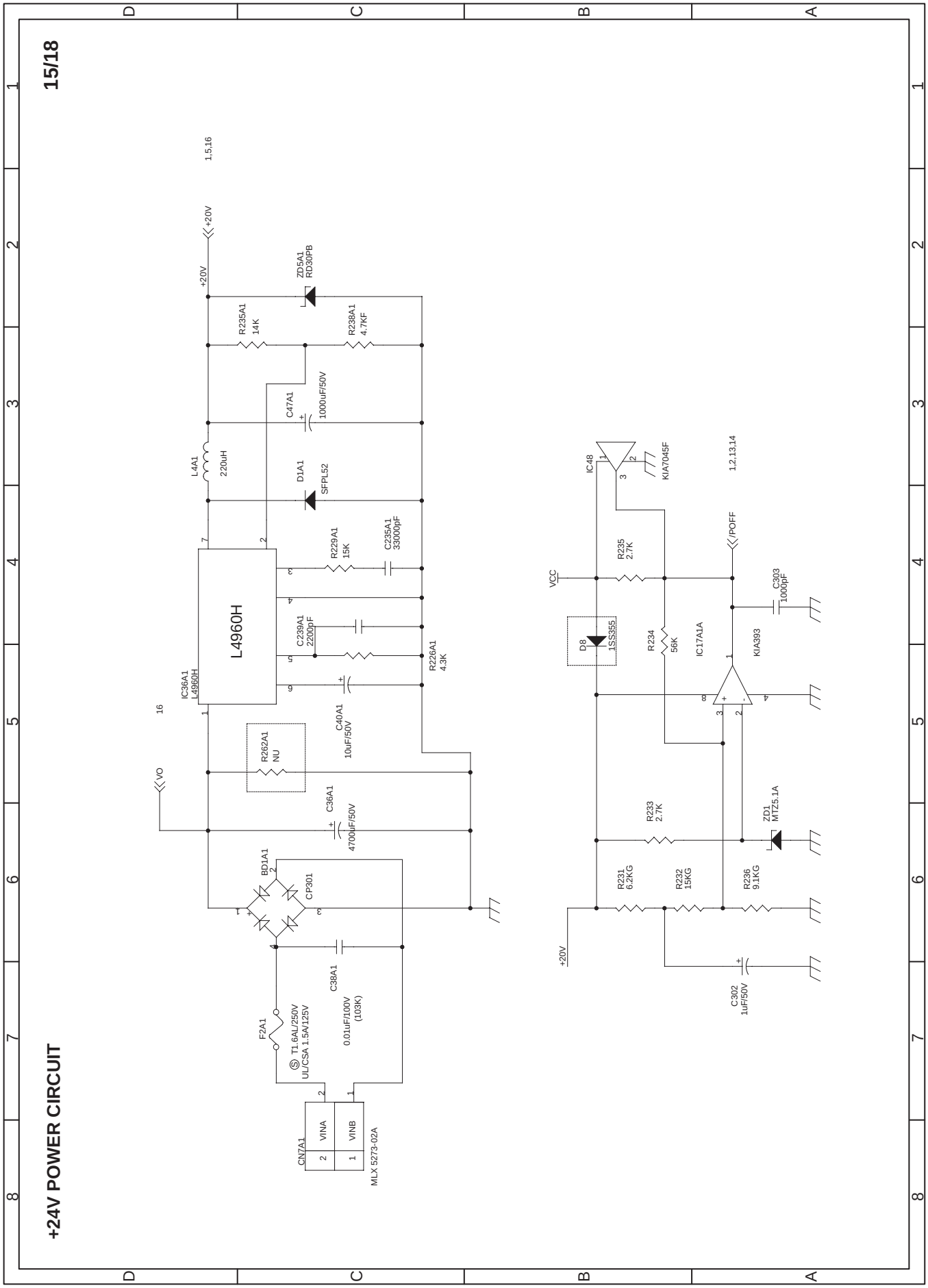

12/18
MEMORY. SCH
IC37
4M EPROM
IC38
LH28F004SUT-NC90
4M FLASH ROM
IC38
HY628100BLLG
1M SRAM
IC35
IDT7134PLCC
DUAL PORT RAM
SW4
R210
10k
R211
10k
R212
10k
R213
10k
R214
0(Not)
R215
0
C274
100pF
C275
100pF
C276
100pF
C277
100pF
C278
100pF
C279
100pF
C280
10uF
C281
0.1uF
C282
10uF
C283
10uF
C284
0.1uF
C285
0.1uF
C286
10uF
C287
0.1uF
C288
0.1uF
VCC
/CSEPROM
/CSFLASH
/CSDPRAM
/IRES
WPH
/MWR
/CER
/MWE
/MRD
LA[0..18]
LD[0..7]
LA[0..11]
LD[8..15]


13/18
MPCA8
IC12
MPCA8
IC11A
IC11B
74LS393
IC23 VCC---GND
IC2314PIN ---VCC
7PIN ---GND
to TOUCH PANEL CON.
VCC
GND
/RES
/VMEM
/RROS1
/VWAIT
/MCRINT
/VRESC
/AS
/RD
/HWR
/IPLON0
/EXWAIT
/WAIT
/UASCK
/TPTRDY
/TPRRDY
/SHEN2
/OPTCS
/INTSW
/INTSR
/WRO
/RDO
/TPRXD
/TPTXD
/TRQ1
/TRQ2
/ROS1
/ROS2
/RCP1
/RCP2
/CLS1
/CLS2
/RDD1
/RDD2
/STH2
/SCK2
/HTS2
/SCK1
/HTS1
/STH1
/POFF
/KRQ
/HTS3
/SCK1
/STH1
/RXDI
/TXDO
/SCKI
/IRQ0
/TPRDY
/RESET
/NMI
/INT3
/INT2
/INT1
/INT0
/EXINT0
/EXINT1
/EXINT2
/EXINT3
/SSPRQ
/SSPSO
/SSPCK
/SSPST
/LCDC
/OPTCS
/INTSW
/INTSR
/WRO
/RDO
/IPLON0
/SHEN2
/TPTRDY
/TPRRDY
/IPLON0
/SHEN2
/EXWAIT
/WAIT
/UASCK
/TPTRDY
/TPRRDY
/IPLON0
/SHEN2
/TPRXD
/TPTXD
/TRQ1
/TRQ2
/ROS1
/ROS2
/RCP1
/RCP2
/CLS1
/CLS2
/RDD1
/RDD2
/STH2
/SCK2
/HTS2
/SCK1
/HTS1
/STH1
/POFF
/KRQ
/HTS3
/SCK1
/STH1
/RXDI
/TXDO
/SCKI
/IRQ0
/TPRDY
/RESET
/NMI
/INT3
/INT2
/INT1
/INT0
/EXINT0
/EXINT1
/EXINT2
/EXINT3
/SSPRQ
/SSPSO
/SSPCK
/SSPST
/LCDC
RASP
RCP2
LCDWT
CLS2
RDD2
TEST2
TEST1
TEST0
STH2
SCK2
HTS2
RCP1
SLMT5
SLMT0
CLS1
RAS3
RDD1
VSS
VCC
ASKCK
SYNC
DOT8
DOT9
RJMT0
RJMT5
DOT5
DOT6
DOT7
VSS
DOT1
DOT2
DOT3
DOT4
TPCKI
TPRXD
TPTXD
RAS2
ROS2
ROS1
OPTCS
EXINT0
EXINT1
EXINT2
EXINT3
WRO
RDO
RA16
VSS
RA17
RA18
EXWAIT
WAIT
MCR2
IPLON
DAX2
PHAI
PIC
IRRX
VSS
VCC
UASCK
UASCK
IRTX
RCO
RCVRDY2
RCVRDY1
TPRDY
TPTRDY
TPRRDY
TEST
MD0
MD1
IPLON
INT4
PRST
PTRG
TRG
A23
RF
IF
ECUT
CUT
VF
STAMP
VIO
VMEM
VSWAP
RES
EROS1
ERQML
INT0
HTS1
SCK1
STH1
MCRINT
VWAIT
VCC
VSS
MCRINT
VRESC
SLTMG
SLRST
AS
RD
WR
PHAI
RASPN1
RASPN1E
RASPN12
VSS
RASPN2
RASPN2E
VCC
SSTI
D0
D1
D2
D3
VSS
D4
D5
D6
D7
SSPRQ
RESET
INT3
RXDI
TXDO
SCKI
IRQ0
A0
A1
A2
A3
A4
A5
VSS
VCC
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
A20
A21
A22
LCDC
MPCA8
A23
R120
R118
R121
R114
R115
R116
R117
R122
R111
R110
R109
R119
R112
R113
R123
C144
C149
C155
C147
C153
C152
C154
C142
C143
C140
C141
C150
C148
C157
C158
C156
C145
C146
C136
C138
C151
C137
C139
C134
C135
X3
7.3728MHz
RCRSP5019BCZZ
680
1M
10K
100pF
330pF
0.1uF
100uF/16V
D[8..15]
A[0..23]
1.6,7,9,14,17 D[8..15]
1.6,7,9,10,12,14,17 A[0..23]
1,2,14,15 /POFF
2 /KRQ
2 /HTS3
2 /SCK1
2 STH1
17 RASPN1
17 RASPN1E
9 /RASPN12
9,17 RASPN2
9,17 RASPN2E
1,7,9 /AS
1,6,7,9,10,12,17 /RD
6,7,9,10,12,17 /HWR
7,9,14 #
1,6,9,10,14 /RES
7 MCRINT
9 /VWAIT
16 VRESC
7 /VMEM
6 /RROS1
7 NMI
1,2,7,17 /RESET
7 /TPRRDY
7 /TPTRDY
7 RXDI
7 TXDO
7 SCKI
7 /IRQ0
11 RCP2
11 CLS2
11 RDD2
11 RCP1
11 CLS1
11 RDD1
1 STH2
1 /SCK2
1 /HTS2
1,14 /OPTCS
1,10 /INTSW
1,10 /INTSR
1,14 /WRO
1,14 /RDO
1,14 /TRQ1
1,14 /TRQ2
1 TPRXD
1 TPTXD
1 VCC
7 /EXWAIT
7 /WAIT
7 /IPLON0
PHAI
7 UASCK
/TPTRDY
/TPRRDY
/IPLON0
1,6,7,9
/SHEN2
1

OPC2

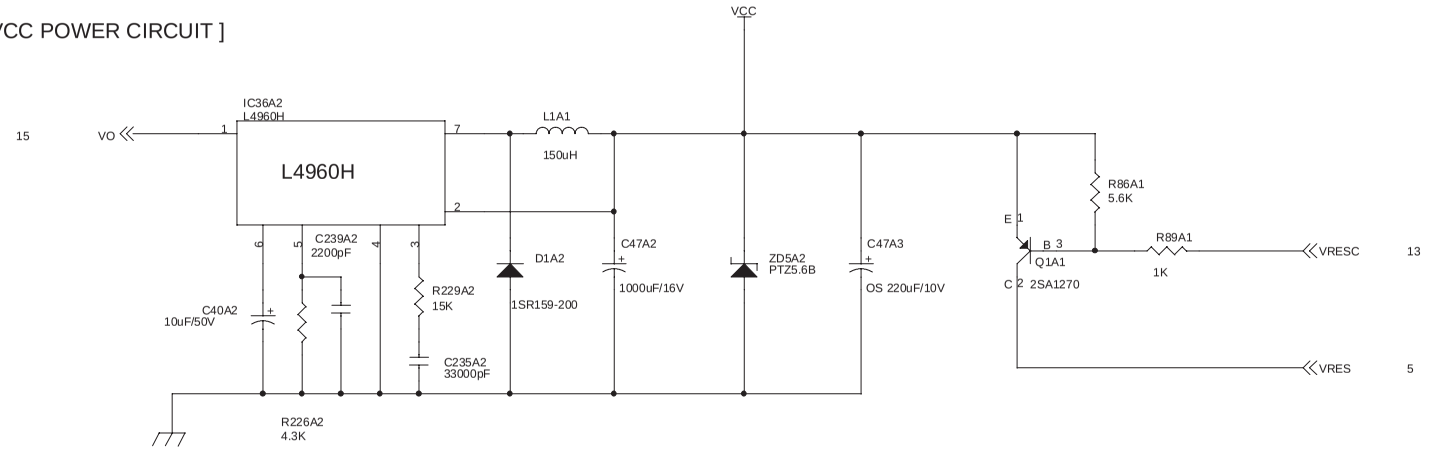
14/18


PLZ BE SHORT PATTERN!
IC13
OPC2
VCC
SL00
SL01
SL02
SL10
SL11
SL12
SL20
SL21
SL22
SL30
SL31
SL32
CD0
BRK0
TRNEMP0
RCVRDY0
TRNRDY0
CTS0
RCVDT0
GND
CI0
RTS0
CS0
CD1
BRK1
TRNEMP1
RCVRDY1
TRNRDY1
CTS1
RCVDT1
CI1
RTS1
CS1
CD2
TRNEMP2
RCVRDY2
TRNRDY2
CTS2
RCVDT2
CI2
CS2
CD3
BRK3
TRNEMP3
RCVRDY3
TRNRDY3
CTS3
RCVDT3
CI3
CS3
D0
D1
D2
D3
GND
D4
D5
D6
D7
GND
VCC
X1
X2
XOUT
TRCK
AB0
AB1
US1CH
PX
POF
RSRQ
TRV
RXDATA0
TXE
TRRQ
TRQ1
TRQ2
A0
A1
MCLK
RST
RSLCT1
RSLCT0
RIN
WIN
SYCBKD
TRNEMPD
RCVRDYD
TRNRDYD
DSRD
CTSD
RCVDTD
RTSD
DTRD
TRNDTD
CSD
GND
VCC
SYCBKC
TRNEMPC
RCVRDYC
TRNRDYC
DSRC
CTSC
RCVDTC
RTSC
DTRC
TRNDTC
CSC
GND
SYCBKB
TRNEMPB
RCVRDYB
TRNRDYB
DSRB
CTSB
RCVDTB
RTSB
DTRB
TRNDTB
CSB
GND
SYCBKA
TRNEMPA
RCVRDYA
TRNRDYA
DSRA
CTSA
RCVDTA
RTSA
DTRA
TRNDTA
CSA
UTST
DBTST
RCVCLK
TRNCLK
RES
GND
VCC
W
R
DB7
DB6
DB5
DB4
GND
DB3
DB2
DB1
DB0
RES
WR
RD
OPTCS
A5
A4
A3
A2
CLK_USART
RES_USART
AH1
AH0
/RDH
/WRH
TRNEMP3
RCVRDY3
TRNRDY3
/DSR3
/RTS3
/DTR3
TXD3
/CS3
BRK2
TRNEMP2
RCVRDY2
TRNRDY2
CLSIN
/CLCOM
CLSOUT
/CS2
BRK1
TRNEMP1
RCVRDY1
TRNRDY1
/DSR1
RCVDT1
/DTR1
TXD1
/CS1
/RES
/WRO
/RDO
/OPTCS
/DCD1
BRK1
TRNEMP1
RCVRDY1
TRNRDY1
/CTS1
RCVDT1
/CI1
/RTS1
BRK2
TRNEMP2
RCVRDY2
TRNRDY2
3 CLSIN
CLSIN
TRNEMP3
RCVRDY3
TRNRDY3
/CTS3
RCVDT3
R125 10K
R238 10K
R124
R126
C161 330pF
C162 330pF
X3
C164
FL1
RCORF6702BHZZ
CLK_USART
C160 10uF/16V
C159 0.1uF
C163 NU
D8
D9
D10
D11
D12
D13
D14
D15
1,6,7,9,13,17 D[8..15]
7,9,13 #
AH0
AH1
1,2,13,15 /POFF
1,7 /IRQ1
1,13 /TRQ2
1,13 /TRQ1
A0
A1
1,6,7,9,12,13,17 A[0..5]

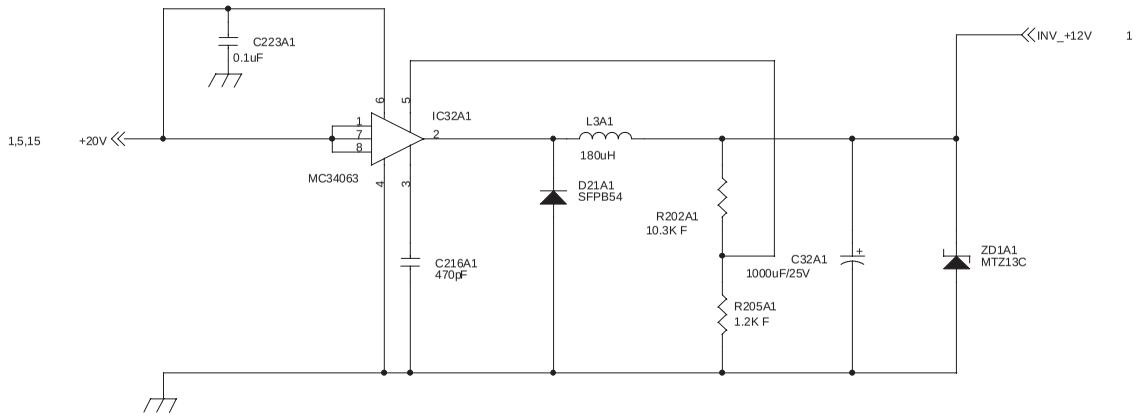

15/18
+24V POWER CIRCUIT
CNTA1
VINA
VINB
MLX 5273-02A
F2A1
T1.6AL/250V
UL/CSA 1.5A/125V
C38A1
0.01uF/100V
(103K)
BD1A1
CP301
C36A1
4700uF/50V
VO
R262A1
NU
C40A1
10uF/50V
IC36A1
L4960H
L4960H
16
C239A1
2200pF
R229A1
15K
C2354A1
33000pF
R226A1
4.3K
L4A1
220uH
D1A1
SFPL52
C47A1
1000uF/50V
R235A1
14K
R238A1
4.7KF
ZD5A1
RD30PB
+20V
1,5,16
+20V
VCC
D8
1SS355
R235
2.7K
IC48
KIA7045F
/POFF
1,2,13,14
R234
56K
IC17A1A
KIA393
C303
1000pF
R233
2.7K
ZD1
MTZ5.1A
R231
6.2KG
R232
15KG
R236
9.1KG
C302
1uF/50V
+20V

VCC/INV_12V CIRCUIT

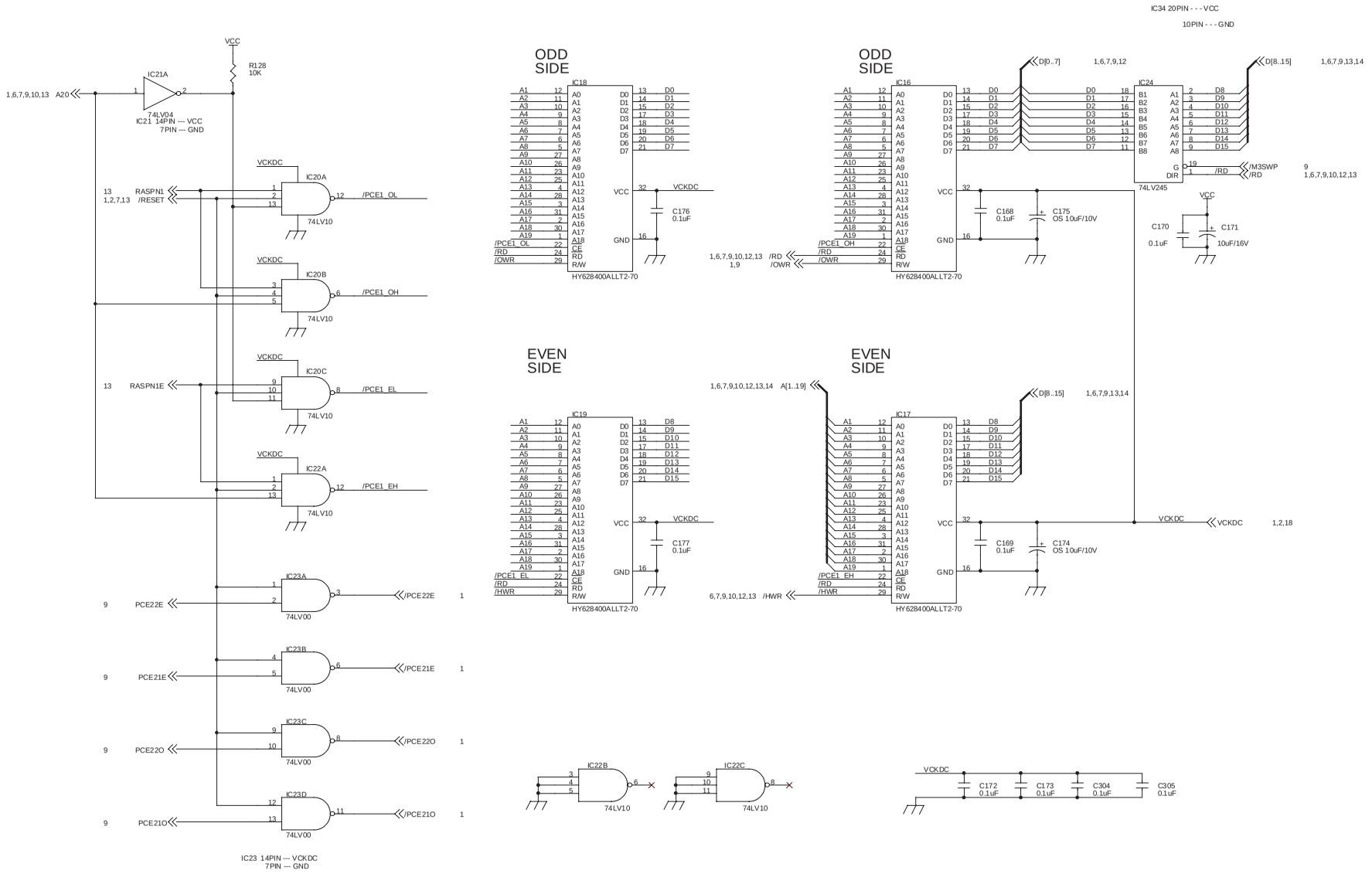
[VCC POWER CIRCUIT]



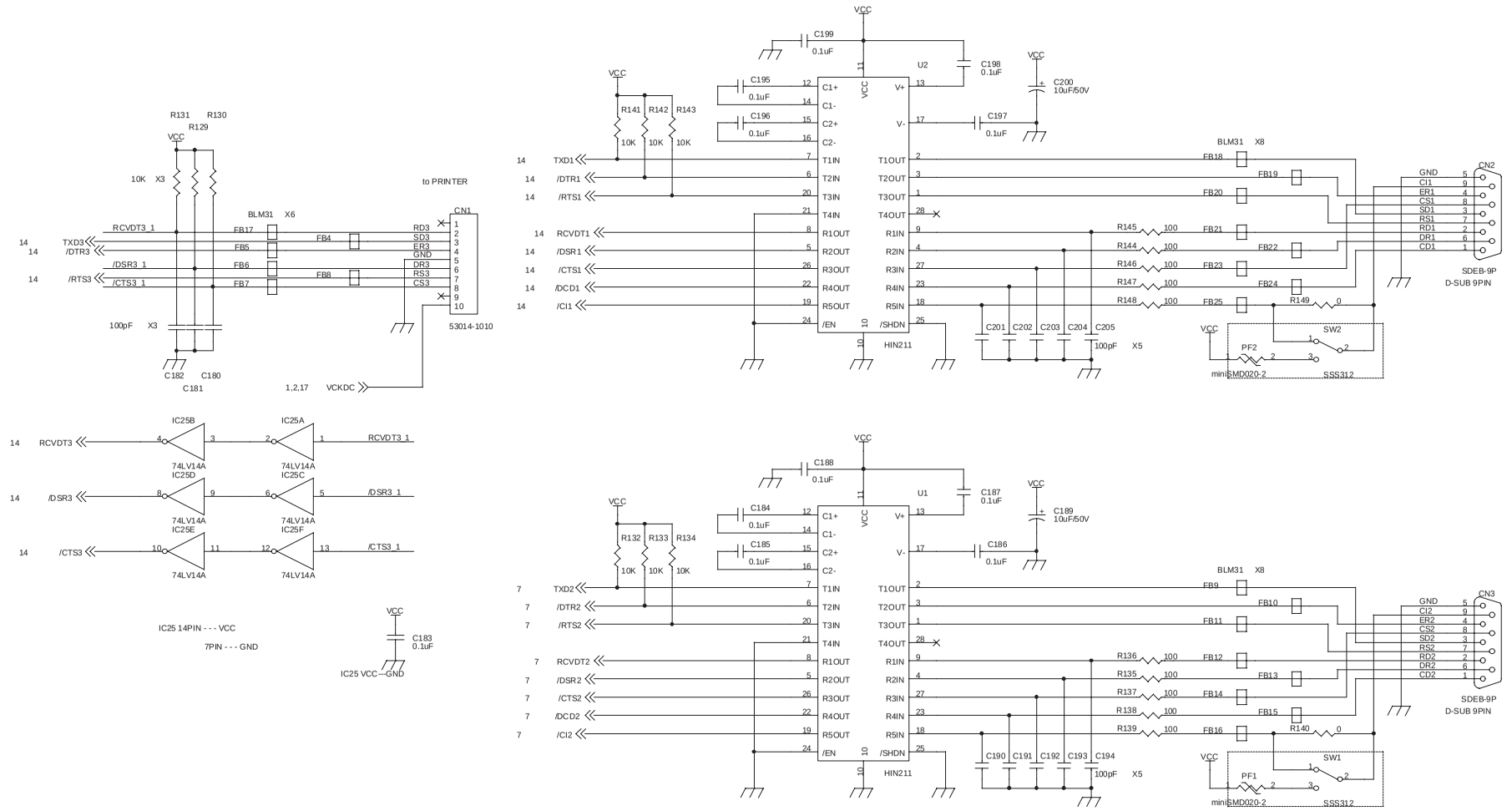
[INV_+12V POWER CIRCUIT]

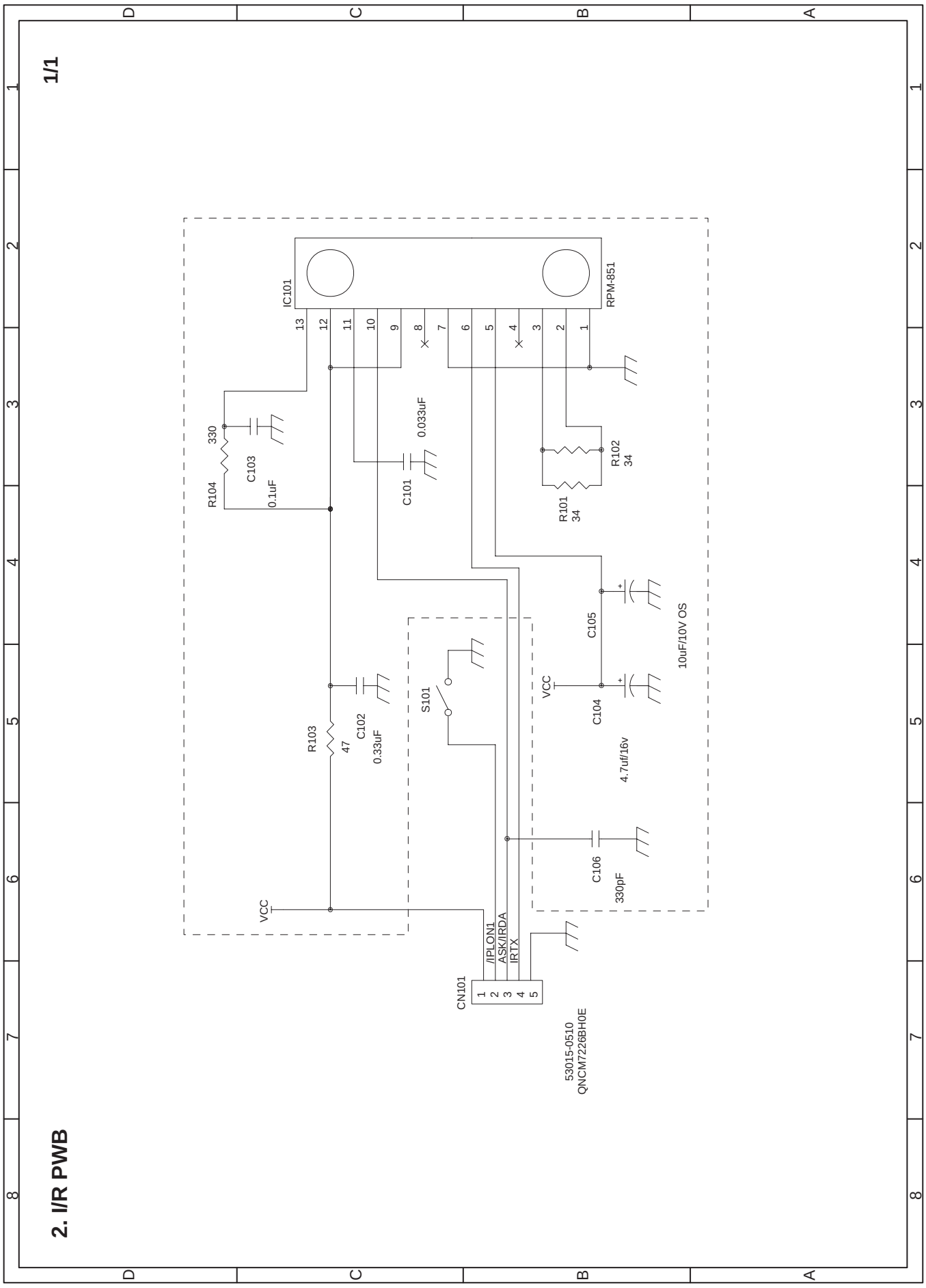


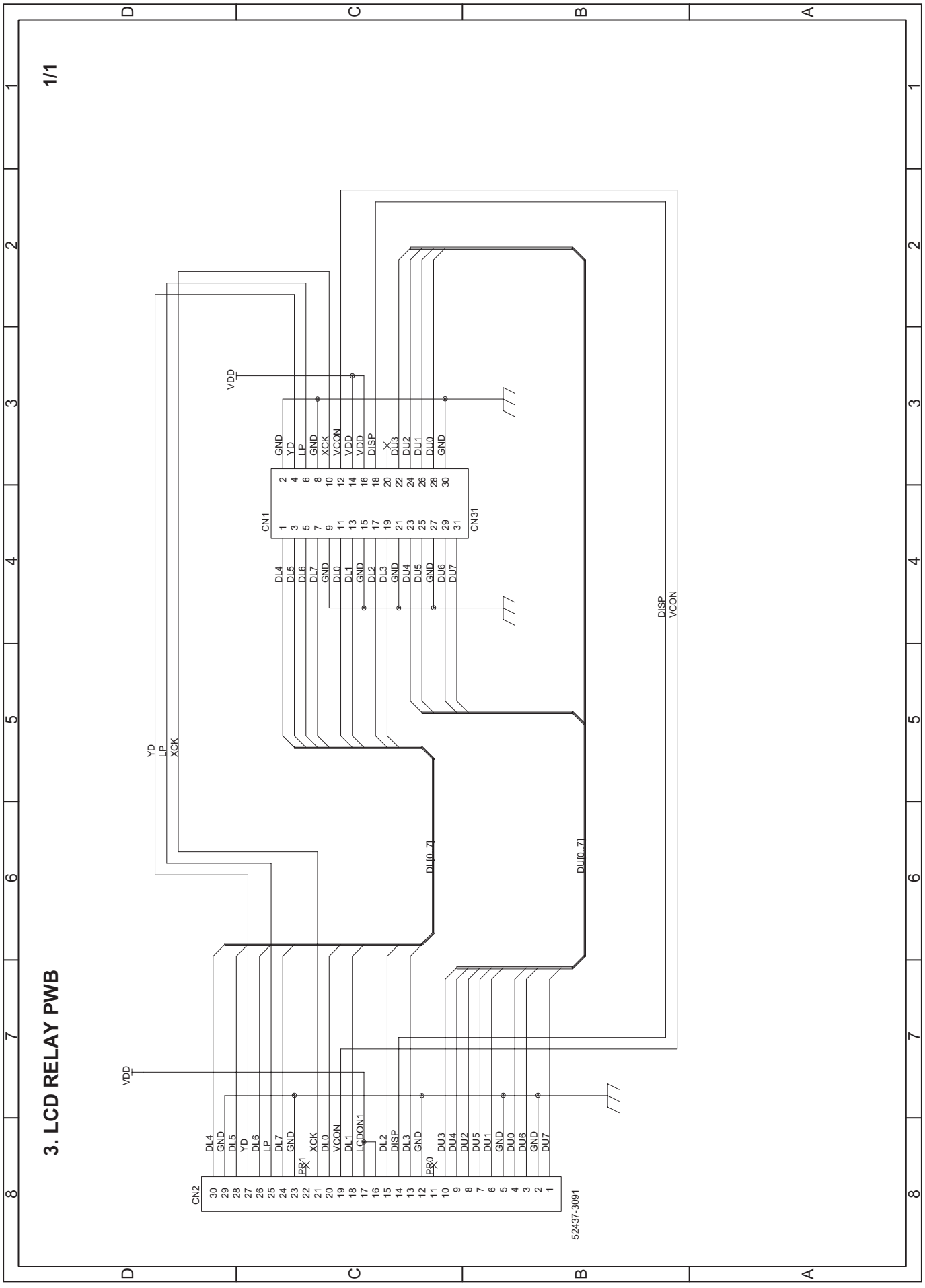
PSRAM

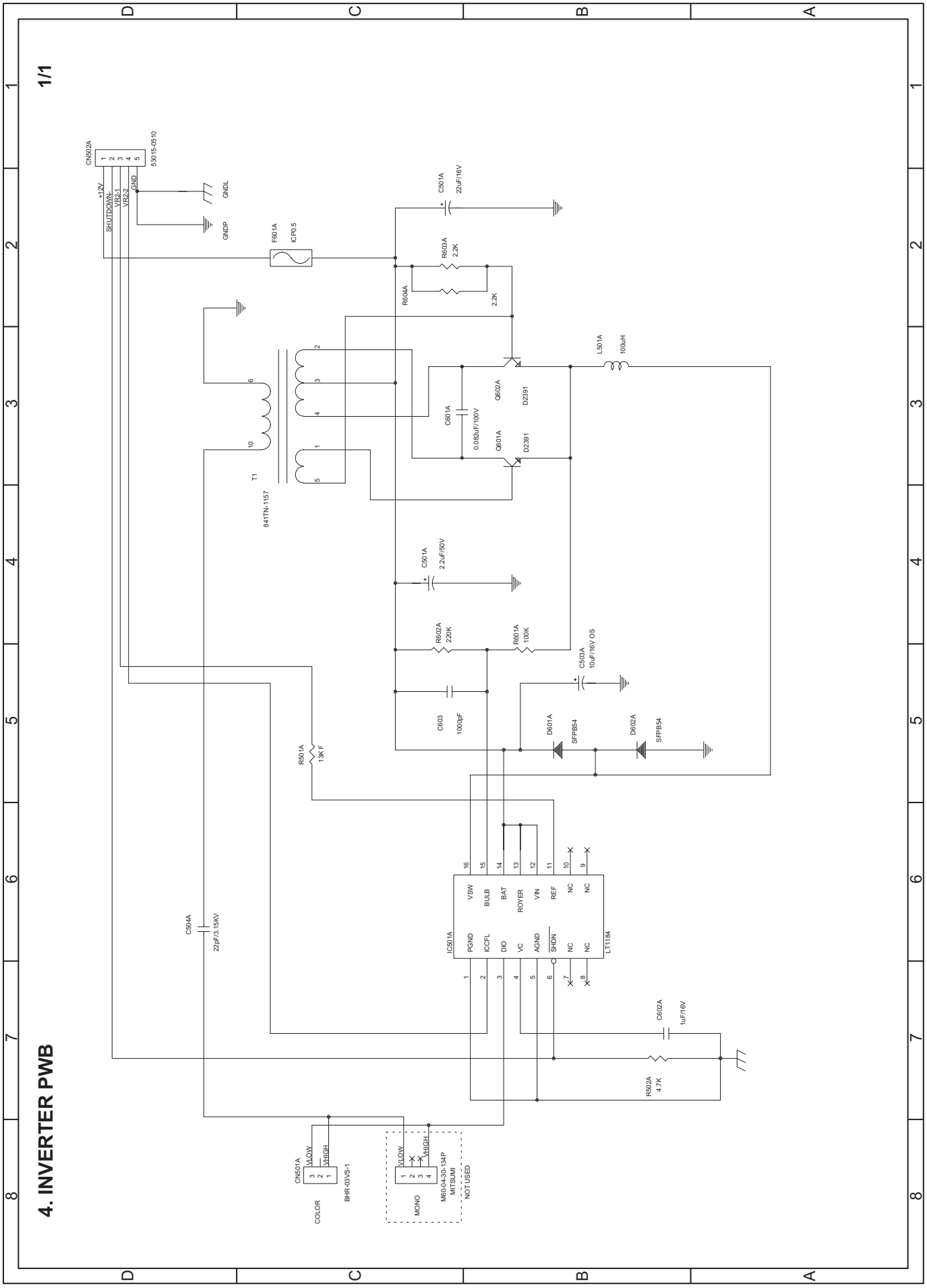

IC34 20PIN - - - VCC
10PIN - - - GND
VCC
R128
10K
IC21A
1,6,7,9,10,13 A20
74LV04
IC21 14PIN --- VCC
7PIN --- GND
VCKDC
IC20A
13 RASPN1
1,2,7,13 /RESET
74LV10
/PCE1_OL
IC20B
/PCE1_OH
IC20C
13 RASPN1E
/PCE1_EL
IC22A
/PCE1_EH
IC23A
9 PCE22E
74LV00
/PCE22E 1
IC23B
9 PCE21E
/PCE21E 1
IC23C
9 PCE22O
/PCE22O 1
IC23D
9 PCE21O
/PCE21O 1
IC23 14PIN --- VCKDC
7PIN --- GND
ODD SIDE
IC18
HY628400ALLT2-70
/PCE1_OL
/RD
/OWR
C176
0.1uF
EVEN SIDE
IC19
/PCE1_EL
C177
0.1uF
IC22B
IC22C
ODD SIDE
IC16
D[0..7] 1,6,7,9,12
/PCE1_OH
1,6,7,9,10,12,13 /RD
1,9 /OWR
C168
0.1uF
C175
OS 10uF/10V
IC24
D[8..15] 1,6,7,9,13,14
74LV245
G
DIR
/RD
/M3SWP
/RD
9
1,6,7,9,10,12,13
VCC
C170
0.1uF
C171
10uF/16V
EVEN SIDE
1,6,7,9,10,12,13,14 A[1..19]
IC17
D[8..15] 1,6,7,9,13,14
/PCE1_EH
6,7,9,10,12,13 /HWR
C169
0.1uF
C174
OS 10uF/10V
VCKDC
VCKDC 1,2,18
C172
0.1uF
C173
0.1uF
C304
0.1uF
C305
0.1uF

RS232


R131
R130
R129
VCC
10K X3
to PRINTER
BLM31 X6
CN1
RCVDT3_1
FB17
RD3
TXD3
/DTR3
FB5
FB4
SD3
ER3
/DSR3_1
FB6
GND
DR3
/RTS3
/CTS3_1
FB7
FB8
RS3
CS3
100pF X3
53014-1010
C182 C180
C181
1,2,17 VCKDC
IC25B
IC25A
RCVDT3
RCVDT3_1
74LV14A
IC25D
IC25C
/DSR3
/DSR3_1
IC25E
IC25F
/CTS3
/CTS3_1
IC25 14PIN - - - VCC
7PIN - - - GND
C183
0.1uF
IC25 VCC – GND
C199
0.1uF
U2
C198
0.1uF
C200
10uF/50V
C195
C196
C197
R141 R142 R143
10K 10K 10K
TXD1
/DTR1
/RTS1
RCVDT1
/DSR1
/CTS1
/DCD1
/CI1
C1+
C1-
C2+
C2-
T1IN
T2IN
T3IN
T4IN
R1OUT
R2OUT
R3OUT
R4OUT
R5OUT
/EN
V+
V-
T1OUT
T2OUT
T3OUT
T4OUT
R1IN
R2IN
R3IN
R4IN
R5IN
/SHDN
HIN211
R145 R144 R146 R147 R148
100
FB18 FB19 FB20 FB21 FB22 FB23 FB24 FB25
R149 0
C201 C202 C203 C204 C205
100pF X5
SW2
PF2
miniSMD020-2
SSS312
GND
CI1
ER1
CS1
SD1
RS1
RD1
DR1
CD1
CN2
SDEB-9P
D-SUB 9PIN
C188
0.1uF
U1
C187
0.1uF
C189
10uF/50V
C184
C185
C186
R132 R133 R134
10K 10K 10K
TXD2
/DTR2
/RTS2
RCVDT2
/DSR2
/CTS2
/DCD2
/CI2
R136 R135 R137 R138 R139
100
FB9 FB10 FB11 FB12 FB13 FB14 FB15 FB16
R140 0
C190 C191 C192 C193 C194
100pF X5
SW1
PF1
miniSMD020-2
SSS312
GND
CI2
ER2
CS2
SD2
RS2
RD2
DR2
CD2
CN3
SDEB-9P
D-SUB 9PIN

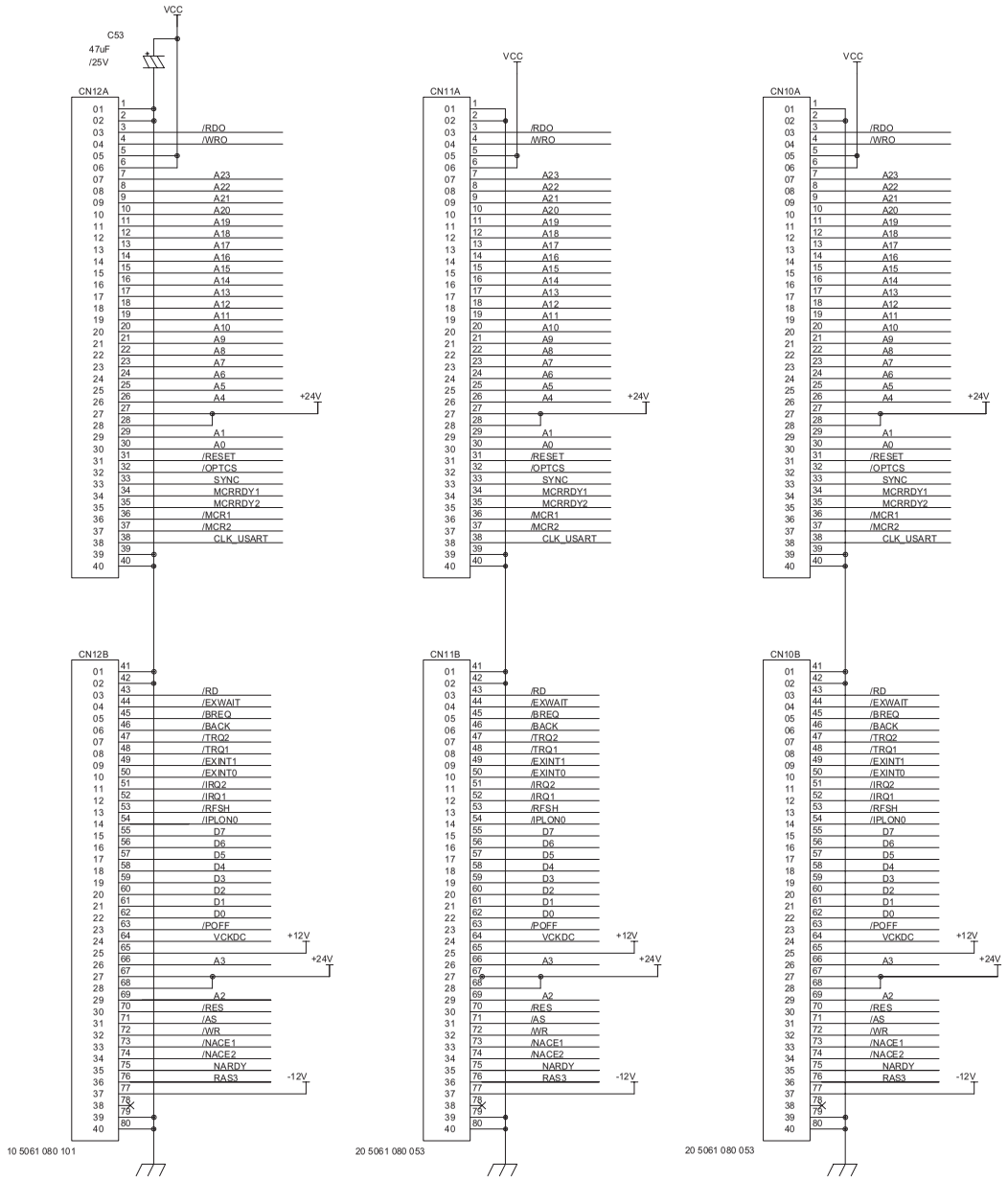

1/1
2. I/R PWB
IC101
RPM-851
13
12
11
10
9
8
7
6
5
4
3
2
1
330
R104
C103
0.1uF
0.033uF
C101
R102
34
R101
34
C105
10uF/10V OS
VCC
S101
C104
4.7uf/16v
R103
47
C102
0.33uF
C106
330pF
VCC
/IPLON1
ASK/IRDA
IRTX
CN101
1
2
3
4
5
53015-0510
QNCM7226BH0E


3. LCD RELAY PWB
1/1
CN2
52437-3091
CN1
CN31
VDD
YD
LP
XCK
DISP
VCON
DLI0_7I
DUI0_7I
LCDON1
PR1
PR0


4. INVERTER PWB
1/1
CN502A
53015-0510
+12V
SHUTDOWN-
VR2-1
VR2-2
GND
GNDL
GNDP
F601A
ICP0.5
C501A
22uF/16V
R603A
2.2K
R604A
2.2K
L501A
100uH
Q602A
D2391
Q601A
D2391
C601A
0.082uF/100V
T1
841TN-1157
C501A
2.2uF/50V
R602A
220K
R601A
100K
C503A
10uF/16V OS
C603
1000pF
D601A
SFPB54
D602A
SFPB54
R501A
13K F
C504A
22pF/3.15KV
IC501A
LT1184
PGND
ICCFL
DIO
VC
AGND
SHDN
VSW
BULB
BAT
ROYER
VIN
REF
NC
NC
NC
NC
NC
C602A
1uF/16V
R502A
4.7K
CN501A
VLOW
VHIGH
BHR-03VS-1
COLOR
MONO
M60-04-30-134P
MITSUMI
NOT USED

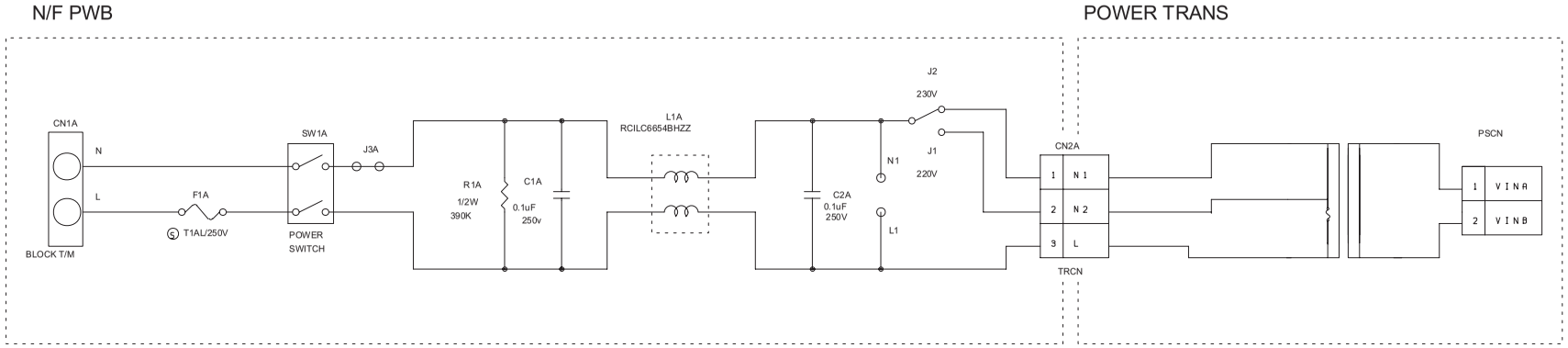
5. MOTHER PWB

1/1



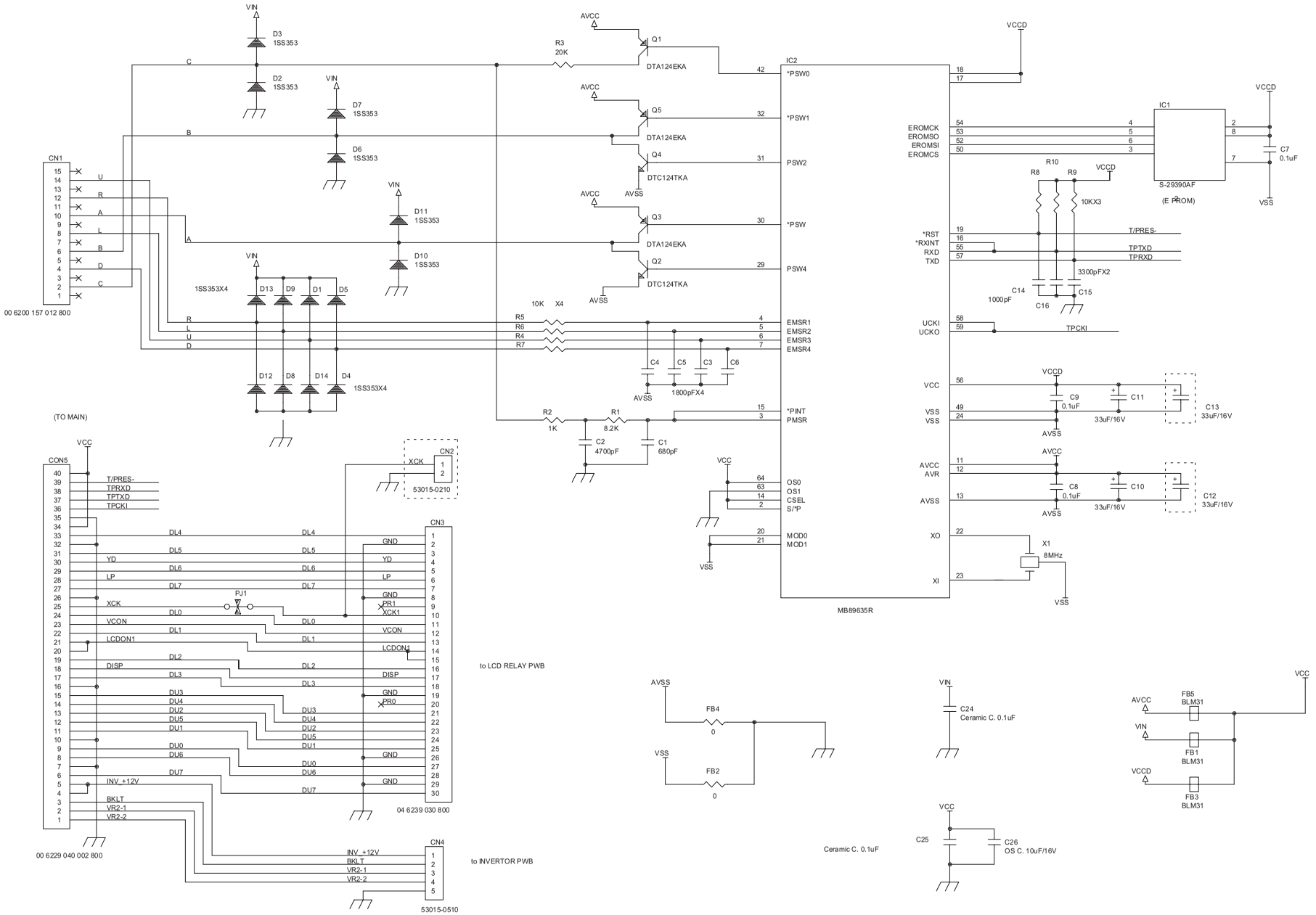
6. N/F PWB UNIT

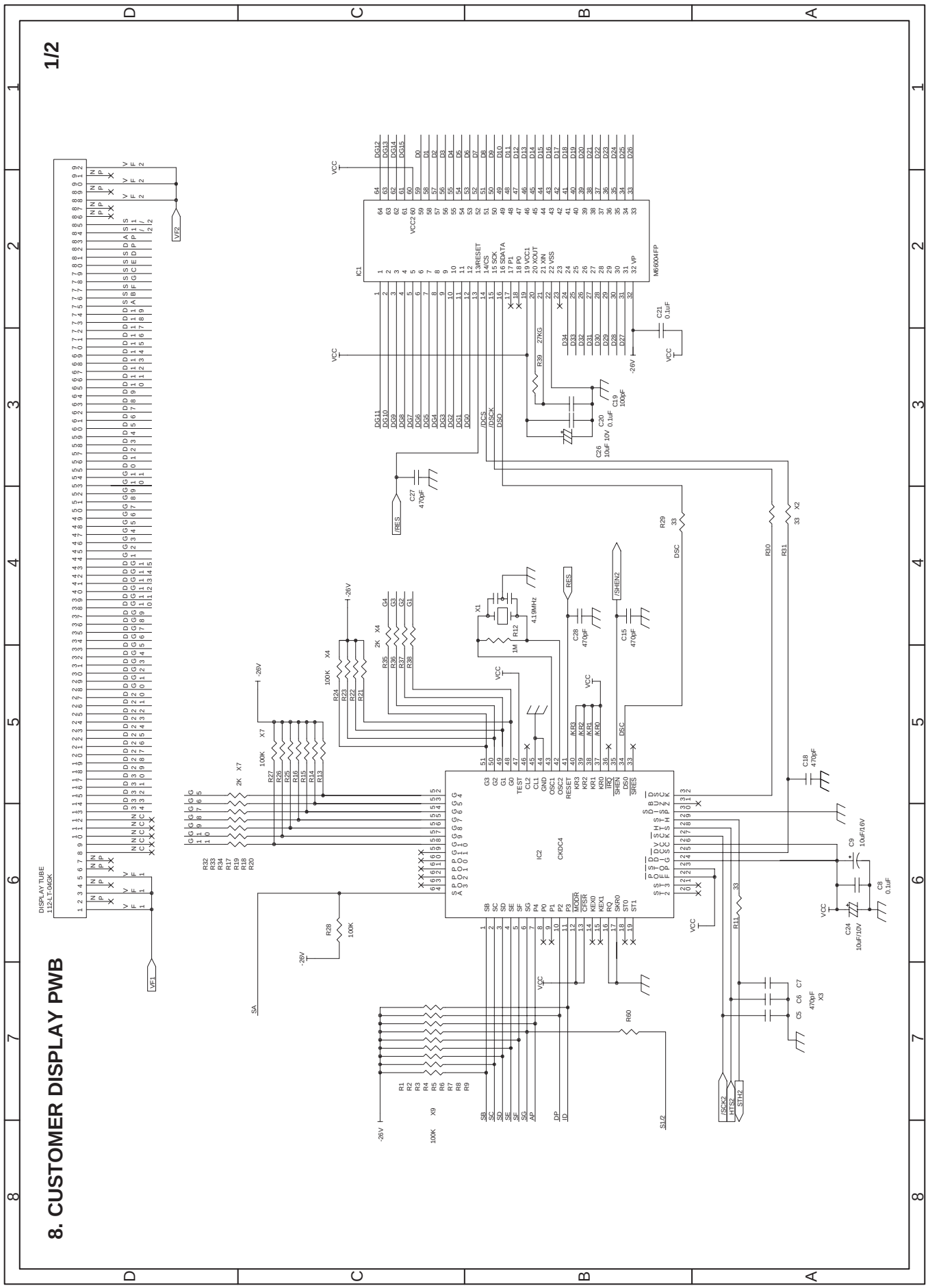
1/1

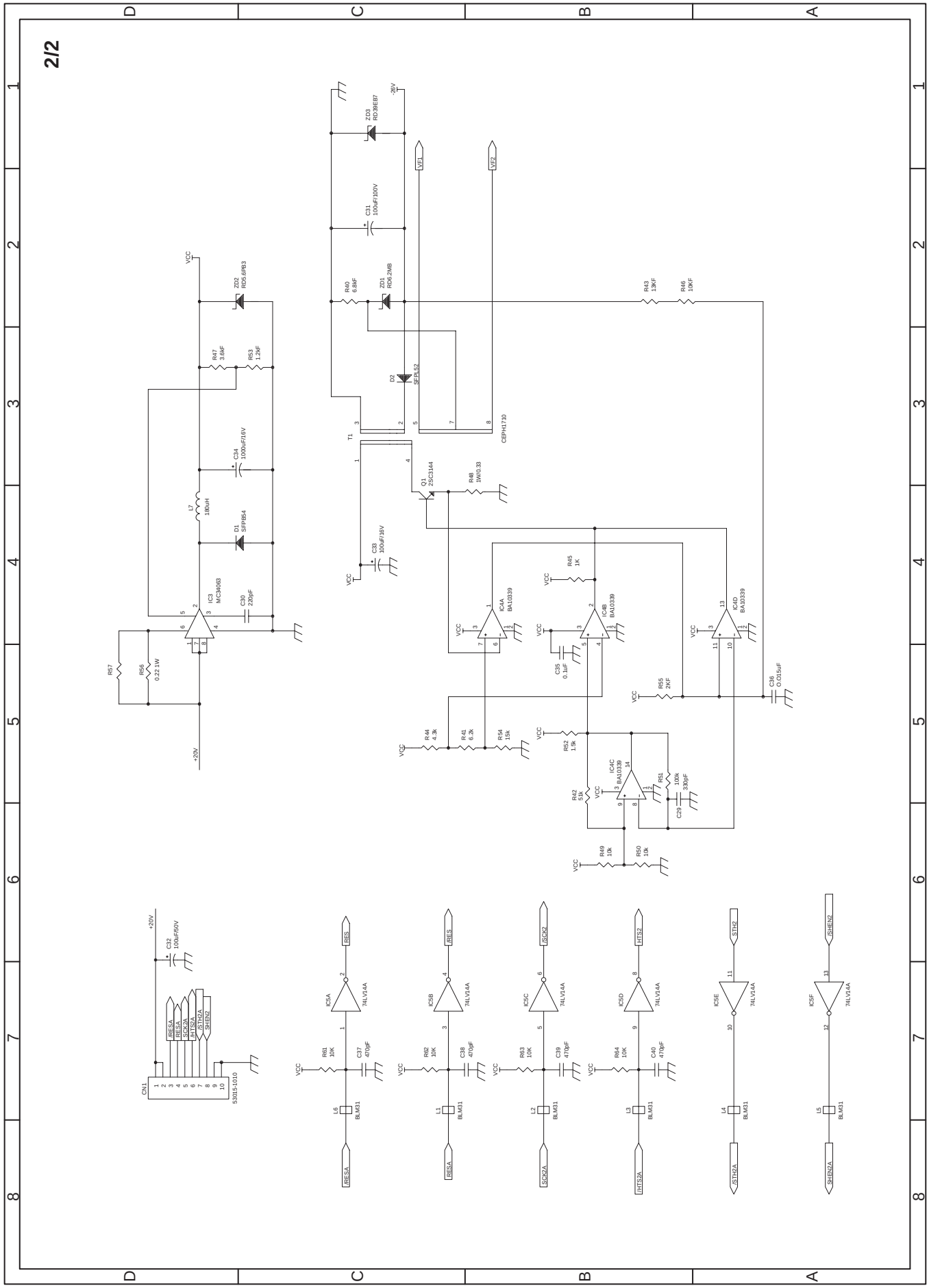


7. TOUCH PANEL PWB

1/1



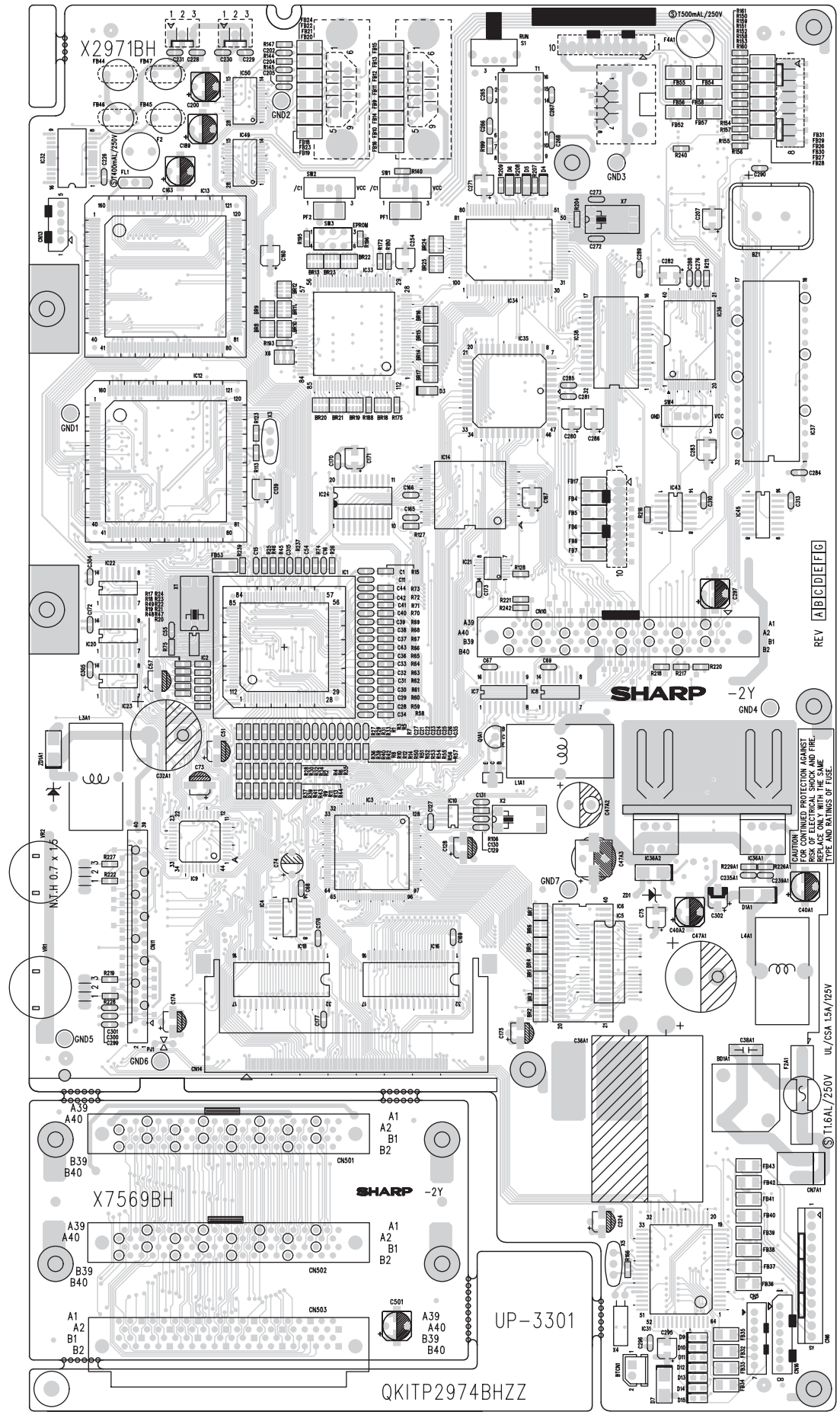

8. CUSTOMER DISPLAY PWB
1/2
DISPLAY TUBE
1121T-T-04Q2K
IC1
M66004FP
IC2
CKDC4
VCC
-26V
4.19MHz
100K
2K
470pF
0.1uF
10uF/16V
10uF/10V
33
/RES
/SHEN2
DSC
/SCK2
HTS2
STH2
SA
SB
SC
SD
SE
SF
SG
AP
DP
ID
SI/2

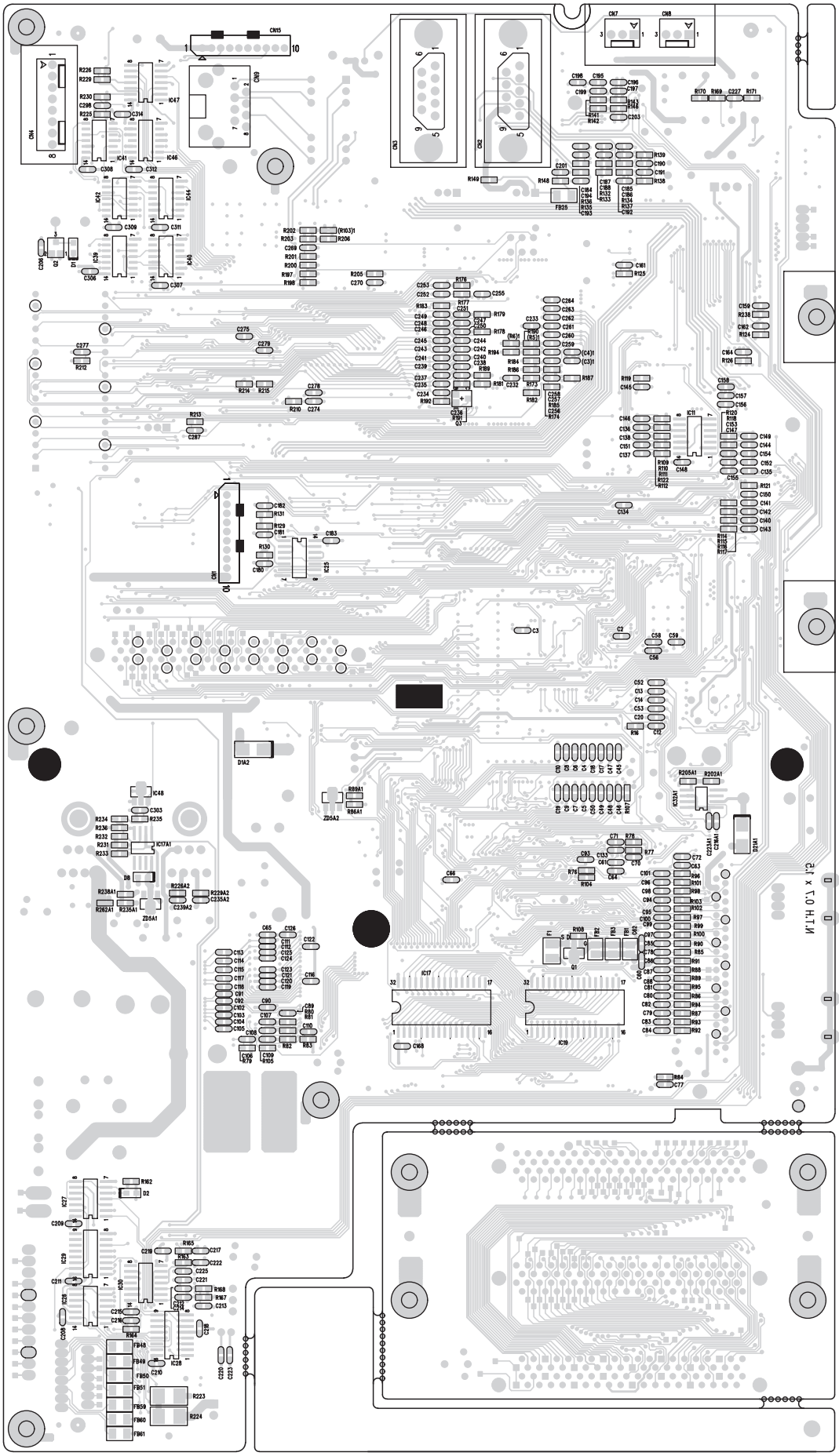

2/2
D
C
B
A
1
2
3
4
5
6
7
8
ZD3 RD-39EB7
-36V
VF1
VF2
C31 100uF/100V
ZD2 RD5.6PB3
ZD1 RD6.2MB
R40 6.8kF
R43 13KF
R46 10KF
R47 3.6kF
R53 1.2kF
D2 SFPL52
T1
CEPH1710
C34 1000uF/16V
L7 180uH
D1 SFPB64
IC3 MC34063
C30 220pF
C33 100uF/16V
Q1 2SC3144
R48 1W/0.33
R57
R56 0.22 1W
+20V
VCC
R45 1K
IC4A BA10339
IC4B BA10339
IC4D BA10339
C35 0.1uF
C36 0.015uF
R55 2KF
R44 4.3k
R41 6.2k
R54 15k
R52 1.5k
IC4C BA10339
R42 51k
R51 100k
C29 330pF
R49 10k
R50 10k
C32 100uF/50V
CN11
53015-1010
/RESA
/SCK2A
/HTS2A
SHEN2
IC5A 74LV14A
IC5B 74LV14A
IC5C 74LV14A
IC5D 74LV14A
IC5E 74LV14A
IC5F 74LV14A
R61 10K
R62 10K
R63 10K
R64 10K
C37 470pF
C38 470pF
C39 470pF
C40 470pF
L6 BLM31
L1 BLM31
L2 BLM31
L3 BLM31
L4 BLM31
L5 BLM31
/STH2
/STH2A
SHEN2A

CHAPTER 9. PWB LAYOUT

1. MAIN PWB

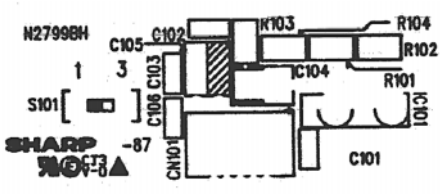
A side





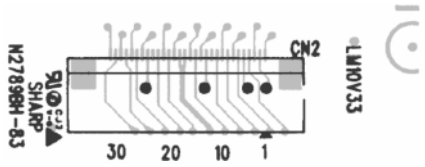
B side

2. IR PWB

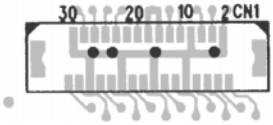


3. LCD PWB

[A Side]

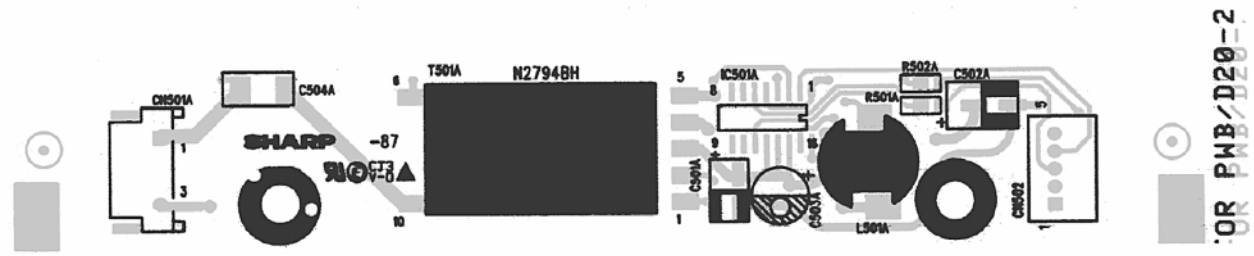


[B Side]



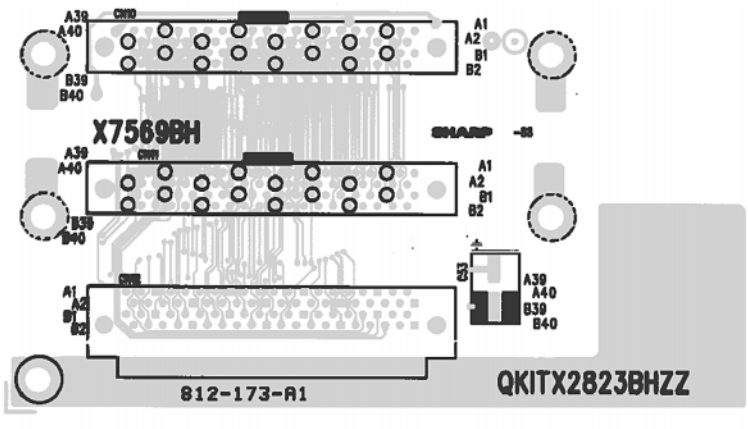
4. INVERTER PWB

[A Side]

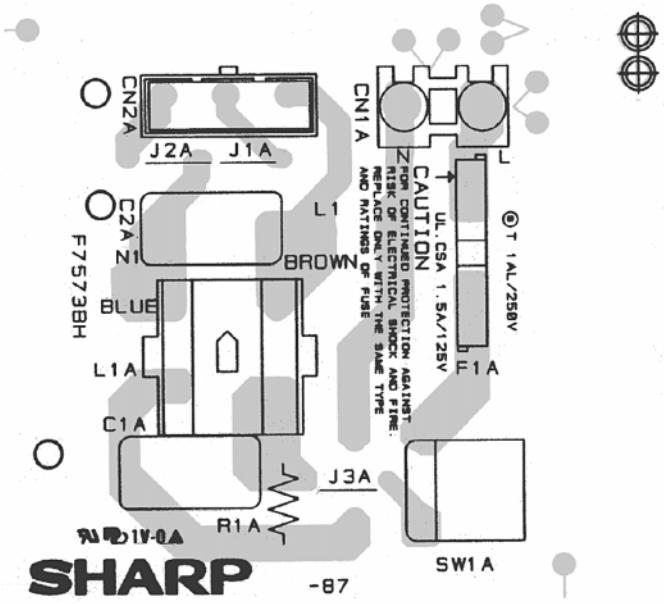


[B Side]

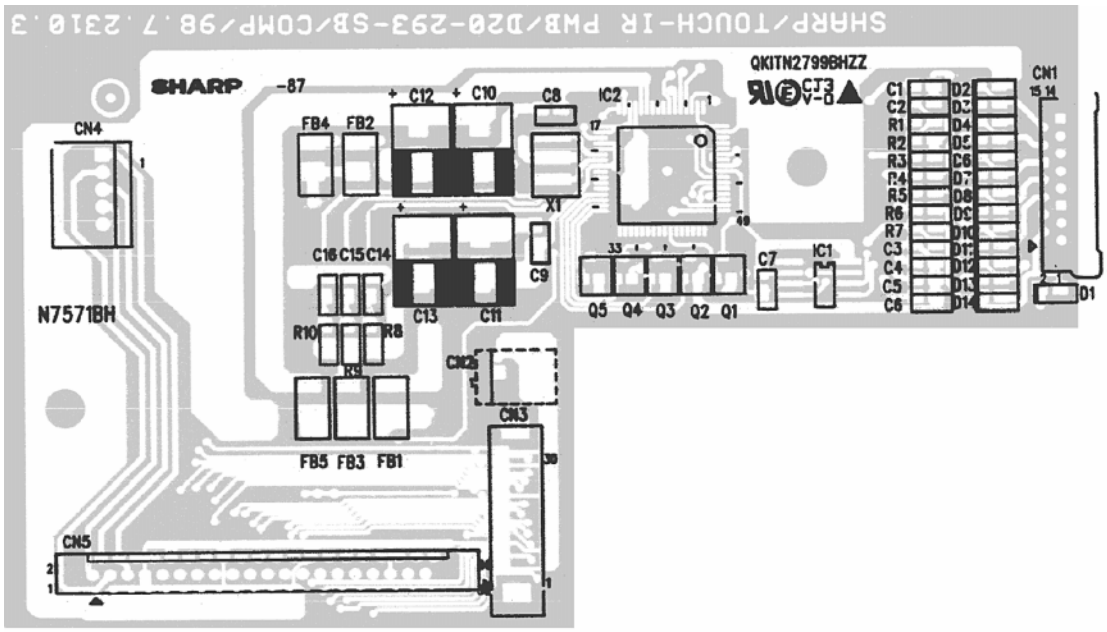
5. MOTHER PWB



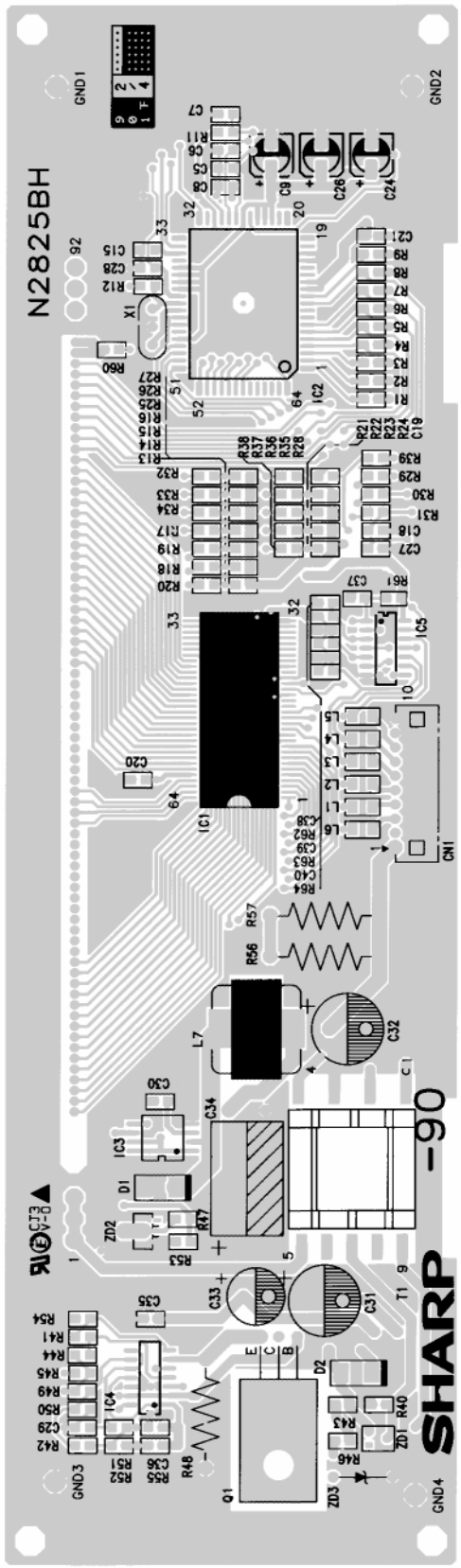
6. N/F PWB



7. TOUCH PANEL PWB



8. CUSTOMER DISPLAY PWB



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